

# Review of Technologies for DC Grids - Power Conversion, Flow Control and Protection

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**Abstract:** This article presents a comprehensive review of dc transmission technologies for future power grids, with particular emphasis on the attributes of the system components that could enhance system controllability and stability, resiliency to ac and dc network faults (fault tolerant operation), and encourage increased exploitation of renewable energy resources for power generation. Detailed discussion of ac/dc and dc/dc converters show that the self-commutated dc transmission system technologies are critical for better utilization of large renewable energy resources which are dispersed over wide geographical areas, while offering the control flexibility needed for proper operation of centralized and decentralized power grids. It is concluded that besides dc voltage matching and power control, the use of expensive and high loss isolated dc/dc converter could be justified in exceptional cases and as part of overall protection systems to prevent dc fault propagation, by splitting large multi-terminal dc networks into several isolated protection zones. Cheaper non-isolated dc/dc converters could be used for dc voltage tapping and matching and power regulation in less critical power corridors, where the loss of control for short periods will not lead to catastrophic impact on system stability (all non-isolated dc/dc converters are unable to prevent a ground potential shift in symmetrical monopole systems). All hybrid dc circuit breakers to date are aimed for fast dc fault isolation, within 3ms to 5ms; while the majority of resonance-based dc circuit breakers with forced current zeros are aimed for relatively slow dc fault clearance times, ranging from 8ms to 12.5ms in an attempt to reduce the cost compared to the former type. Series type dc power flow controllers offer the cheapest way to optimize power flow in highly meshed dc networks.

## 1. INTRODUCTION

Renewable power generation has increased substantially in all major developed and developing countries, presenting significant challenges to grid operators at generation, transmission and distribution levels. Some of these challenges can be summarised as follows [1-6]:

- Wide spread uses of HVDC links and wind generators with fully rated back-to-back converters deprive ac grids from the contribution of the generators' rotating inertias to damping of low frequency power oscillations following major ac network disturbances.
- Intermittent nature of renewable energy resources exacerbates the problems of power balance and poor utilization of the ac lines due to undesirable power flow in ac power systems with high penetration of renewable power generation.
- Operation of power electronic based solar and wind generators, which are less sensitive to frequency variation ( $\pm 2.5$ Hz) alongside the frequency sensitive large conventional synchronous generators, render most existing protection philosophies inadequate. This is because the stability margins of the latter dictate the overall stability of the entire power system, leading to unnecessary loss of generation or tripping of conventional power plants due to loss of synchronism.

Some of these challenges could be addressed with well-designed smart grids that employ both ac and dc transmission systems with state-of-arts control and communication systems, where the vast energy stored in the dc lines and converters' cell capacitors of the asynchronous connections could be manipulated to mitigate the effect of renewable energy

resources variability on power quality, and improve transient stability by splitting large ac power systems into several independent asynchronous ac protection zones in order to prevent ac fault propagation throughout the system [4, 5, 7]. In this manner, conventional synchronous and doubly fed induction generators can contribute to power oscillation damping (POD) in their respective zone alongside the synthetic inertia from the capacitors of asynchronous links. The trend of data driven power consumption at lower distribution systems of smart grids (380~415V) may require agile generation and transmission system infrastructures which are able to cope with rapid change in power demand, mainly driven by electricity prices, consumer behaviour, and other autonomous smart devices for demand side management [8-11]. To avoid poor utilization of the generation and transmission infrastructures in data driven smart grids, fast and secure communication systems capable of dealing with large data and a number of high level controllers will be required to optimize the power flow at the transmission level. This flow optimisation can be done with:

- converter terminals of the HVDC interconnectors
- embedded HVDC links within some of the ac protection zones
- flexible ac transmission system (FACTS) devices
- high-voltage dc-dc converters, which manage the power flow in meshed parts of the dc infrastructure

Instead of the present large centralized power grids, centralized operation of large smart grids that spread over wide areas such as Europe, USA, China and India are necessary for better utilization of the diversity of renewable energy resources across different regions; thus, leading to provision of cheap, reliable and sustainable power throughout all four seasons of the year. In this manner, power plant types which are operated with fixed output power such as nuclear and other fossil fuel

based plants could be reduced [10, 12-17]. In contrast, the planned transition of smart grids from centralised to decentralised operation could be executed during major network faults or outages of the critical power corridors, with no or minimum loss of power supply, provided the said ac protection zones are designed to be self-contained (each must be able to satisfy the grid code as an independent ac network). In being able to operate in centralised and decentralised modes, smart grids have potential to avoid the problem of total system blackout.

The multi-terminal HVDC transmission network concept is attractive to many transmission system operators, and for future smart grids because of the following reasons:

- real power can be exchanged over a wide geographical area at reduced transmission power loss
- increased control flexibility over power flow (magnitude and direction) using a reduced number of converters and dc cables (hence, offers cost-effective solution)
- dc line conductor cross-section areas are fully utilized for carrying real power (no parasitic current or reactive current)
- dc line loadability is not limited by its surge impedance loading (SIL) as in equivalent ac lines, and dc lines are magnetic field neutral (less harmful to nearby wildlife and sea creatures)

However, because of low resistance and rapidly diminishing effect of the line inductance during a dc short circuit fault, the speed of dc fault propagation is much faster than an ac fault. Also, because the dc fault current increases rapidly within the first 3ms of the fault initiation, the dc short circuit fault has to be interrupted within an ac sub-fundamental cycle to avoid irreparable damage to expensive and vulnerable part of the dc network, such as power converters. Recently, significant effort has been invested in the development of new types of power converters that do not increase the fault level in the dc network and can survive dc faults for extended periods (several milliseconds without the risk of damage). This has been done in an attempt to relax dc circuit breakers requirements (in terms of let-through current, current breaking capacity, and operating speed). Although some of the emerged converters and dc circuit breakers are designed to cope with the high demands of dc faults, most of these circuit breakers require a number of sizable extra dc inductors to be incorporated into the dc-link or converter control modification to slow down the rate of rise of the dc fault current at the dc-link of each converter and rate of fall of the dc-link voltage or actively control the fault current [1, 3, 10, 18, 19]. Research is needed into protection aspects related to fault detection and discrimination and in coordination between ac and dc side protection to avoid catastrophic outcomes of miss-operation.

This discussion shows that besides complex control and communication systems, line and self-commutated FACTS devices and HVDC transmission systems and high-voltage dc-dc converters are all critical in achieving the increased control flexibility expected from smart grids. Besides increased controllability, smart grids provide platforms to facilitate a cheap way to integrate many renewable power plants into power grids, without the need for energy storage systems, benefiting from the diversity of renewable energy resources in different regions. Therefore, this paper presents a comprehensive review of the transmission system technologies for smart grids, with particular focus on components of dc transmission systems. Although a qualitative discussion is used

as the main tool to articulate the attributes and limitations of different components or solutions in general and from a smart grid prospective, quantitative substantiation is used in a limited number of cases.

## 2. MODULAR MULTILEVEL AC-DC CONVERTERS

Fig. 1 shows the modular multilevel converter [20-27]. Each phase-leg of the MMC comprises of upper and lower arms, and each arm consists of ' $N$ ' cascaded cells such as in Fig. 1, and must support the full dc-link voltage ' $V_{dc}$ '. The voltage across each cell capacitor must be regulated around  $V_{cell}=V_{dc}/N$  or  $V_{cell}=V_{cref}/N$ , depending on the control method employed. Correct operation of the MMC is achieved when each of phase-leg inserts a sufficient number of cell capacitors into conduction path to counter the input dc-link voltage, and this imposes complementary operation of the upper and lower arms of the same phase-leg according to the following insertion functions:

$$n_{a1}(t) = \frac{1}{2} N_1 [\alpha_d - m \sin(\omega t + \delta)] \quad \text{and} \\ n_{a2}(t) = \frac{1}{2} N_1 [\alpha_d + m \sin(\omega t + \delta)]; \quad \text{where, } \alpha_d = V_{dc1}/V_{cref} \text{ is the}$$

dc modulation index,  $m$  is the ac amplitude modulation index,  $\delta$  is arbitrary load angle,  $V_{cref}$  is the desired set-point for the sum of the cell capacitor voltages of each arm, and  $n_{a1}$  and  $n_{a2}$  are the number of cells to be inserted into the power path from the upper and lower arms at each instant. Instantaneous voltage across the upper and lower MMC arms are:

$$v_{a1} = n_{a1}(t) \times V_{cell} = \frac{1}{2} V_{cref} [\alpha_d - m \sin(\omega t + \delta)] \quad \text{and} \\ v_{a2} = n_{a2}(t) \times V_{cell} = \frac{1}{2} V_{cref} [\alpha_d + m \sin(\omega t + \delta)] \quad [18, \quad 28].$$

Considering phase ' $a$ ' as an example, MMC terminal phase voltage ( $v_{ao}$ ) at output ' $ao$ ' relative to ground ( $O_I$ ) represents the different-mode voltage of phase-leg ' $a$ ' and is given by:

$$v_{ao1} = v_{a2} - v_{a1} = \frac{1}{2} m V_{cref} \sin(\omega t + \delta). \text{ During normal operation, } V_{cref} \text{ is regulated around } V_{dc}; \text{ thus, } \alpha_d \approx 1. \text{ This operation}$$

allows each MMC phase leg to present sufficient dc or common-mode voltage ( $v_{a1}+v_{a2} \approx \alpha_d V_{cref}$ ) to counter the input dc-link voltage ( $V_{dc1}$ ), while maintaining a small voltage mismatch between the two voltages to allow the dc current flow; thus, power exchange between the ac and dc sides. The arm inductor  $L_d$  in Fig. 1 limits the inrush current due to mismatch between common-mode voltage and input dc-link voltage. This operation means the MMC is the only VSC where the upper and lower arms of the same phase leg conduct simultaneously; with arms containing continuous ac and dc currents. The fundamental components of the arm currents are used to exchange active power between the converter and ac sides, while the dc components of the arm currents provide power transfer from the converter to the dc side [29]. When  $i_{a1}$  and  $i_{a2}$  are phase ' $a$ ' upper and lower arm currents as defined in Fig. 1, phase ' $a$ ' output current ( $i_{ao}$ ) represents the differential-mode current ( $i_{ao}=i_{a1}-i_{a2}$ ). The current component that circulates between the upper and lower arm of phase ' $a$ ', without reaching the output circuit, is denoted as common-mode current ' $i_{com}$ ' and is given by:  $i_{com}=\frac{1}{2}(i_{a1}+i_{a2})$ . Without dedicated active or passive countermeasure, the MMC arm or common-mode currents may contain some parasitic components such as 2<sup>nd</sup> order harmonic current that could increase semiconductor losses and cell capacitor voltage ripple. The main attributes and drawbacks of MMCs are [20-27]:

- The MMC generates sinusoidal output voltages, with near zero harmonics and extremely low voltage stresses ( $dv/dt$ )

on the interfacing transformer; thus, ac filters and phase interfacing reactors are not needed.

- Beside the known attributes of conventional voltage source converters {xx}, the circuit structure of the MMC permits the power rated and dc operating voltage of VSC-HVDC links to be increased to a level comparable to that of conventional of LCC-HVDC links; and internal fault management, which is necessary for continued operation during cell failure (cell capacitors or switching devices). Moreover, the use of distributed cell capacitors in MMCs reduces the first peak (or transient component) of the let-through currents that may flow in the dc circuit breaker before its opening; thus, allowing dc circuit breaker design requirements to be relaxed.

However, the large footprint of the MMC due to the use of a large number of cell capacitors, represents a major drawback from the scenery point of view and costs of right-of-way. The ratings for MMCs have reached 1000 MW and 525 kV [30].

The properties of the MMC highly depend on the internal structure of the utilised cells. The following subsections give an overview on the most prominent proposed cell types.

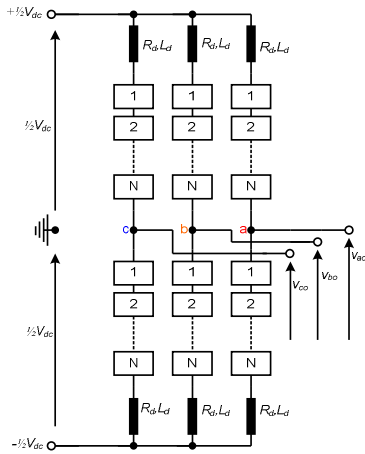


Fig. 1: Schematic diagrams of the generic MMC

### 2.1 Half-bridge cell MMC (HB-MMC)

Fig. 2 (a) shows a half-bridge cell [23, 25, 26]. The HB-MMC offers low semiconductor losses, which is in line with the decarbonisation efforts of transmission networks; but is subject to the same constraints of conventional VSCs such as operation with unipolar dc-link voltage and vulnerability to dc faults. All existing MMC-type HVDC links currently operational are HB-MMCs.

### 2.2 Full-bridge cell MMC (FB-MMC)

Fig. 2 (b) shows a full-bridge cell. Although the FB-MMC has high semiconductor losses, it offers dc fault reverse blocking capability; and operation with variable and bipolar dc-link voltage, including zero dc voltage, while retaining full control over active and reactive power exchange between converter ac and dc sides [31-33]. This feature means the FB-MMC handles dc faults without the need to block the converter, while full control over the ac current in-feed from the ac side is retained. Additionally, bipolar dc voltage operation allows the FB-MMC to operate in a generic dc grid, side by side to line commutated converters (as the FB-MMC can change power flow direction with the change of dc current or dc voltage polarities). These attributes are expected to be invaluable in the delivery of increased control flexibility needed in smart grids.

FB-MMC technology has been proposed for a HVDC link with overhead lines in Germany: the ULTRANET project ( $\pm 380$  kV, 2 GW) [34]. The main reason for applying full-bridge technology was better fault handling ability, since the project uses overhead lines, where the likelihoods of DC faults are much higher compared to its counterpart with cables.

### 2.3 Doubled clamped cell MMC (DCL-MMC)

Fig. 2 (c) shows a three-level double clamped cell. Each cell of the DCL-MMC is equivalent to two HB cells as it uses two capacitors and generates three viable voltage levels ( $2V_c$ ,  $V_c$  and  $0$ ) provided the cell capacitor ( $C_1$  and  $C_2$ ) voltages are maintained such that  $V_{c1} \approx V_{c2} \approx V_c$  (this is contrary to that explained in [35]). But each double clamped cell in Fig. 2(c) inserts three semiconductor switching devices in conduction path, instead of two switches with equivalent HB cells but offers dc fault reverse voltage blocking capability, lacked in the HB-MMC. The main weaknesses of the DCL-MMC are:

- The inability of DCL cell to generate a negative voltage level for both polarities of arm current restricts its operation to unipolar dc-link voltages. Thus it is unable to facilitate operation with a reduced dc-link voltage, unlike the MC-MMC.
- Activation of dc fault blocking capability (switching off all IGBTs) creates a special state where the two capacitors of each DCL cell are connected in parallel. This may create a large surge current due to the voltage difference between capacitors  $C_1$  and  $C_2$ , depending on the current-limiting resistances in series with diodes  $D_1$  and  $D_2$ .

### 2.4 Five-level cross-connected cell MMC (5LCC-MMC)

Fig. 2 (d) shows a symmetrical five-level cross-connected cell that can generate voltage levels  $2V_c$ ,  $V_c$ ,  $0$ ,  $-V_c$  and  $-2V_c$ , provided the cell capacitor voltages are regulated such that  $V_{c1} \approx V_{c2} \approx V_c$  [35]. The five-level cross-connected cell in Fig. 2 (d) is equivalent to two symmetrical full-bridge cells (four devices in conduction path, generate the same voltage levels); thus, its loss performance and control range and flexibility is expected to be similar to that of the FB-MMC, including operation with positive and negative dc-link voltages.

### 2.5 Flying capacitor cell MMC (FC-MMC)

Fig. 2 (e) shows a half-bridge flying capacitor unipolar cell, where each cell generates three voltage levels  $0$ ,  $V_c$  and  $2V_c$  [35]. This flying capacitor cell is equivalent to two half-bridges, where both insert two switches in the conduction path, but uses two capacitors rated at different voltages ( $2V_c$  and  $V_c$ ), compared to  $V_c$  in the equivalent HB cells. Therefore, the FC-MMC is expected to be subject to the same control range limitations as the HB-MMC and unipolar dc-link voltage operation and lack of dc reverse blocking. Capacitors with different rated voltages compromises power circuit modularity, thus is less attractive in terms of cell manufacture and maintenance. Although the FC cell can be configured as a symmetrical bipolar cell, similar to FB and five-level cross-connected cells described previously, this possibility is unattractive due to large number of cell capacitors required.

### 2.6 Active neutral-point clamped unipolar cell MMC (ANPC-MMC)

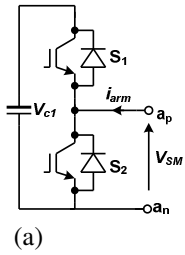
Fig. 2 (f) displays the modular multilevel converter that uses an active neutral-point-clamped unipolar cell to generate

three voltage levels per cell ( $0, V_c$  and  $2V_c$ ) [35]. Operationally, the control range of an ANPC-MMC is limited to unipolar positive dc-link voltages as with the HB-MMC, where power reversal is only achieved by changing the polarity of the dc-link current, and it is unable to block dc faults or decouple cell capacitor regulation from the dc-link voltage ( $V_{dc}$ ) over a wide range; especially, when  $V_{dc}$  falls below the peak of the line-to-line voltage the interfacing transformer imposes at the converter terminals. Because of the lack of redundant switch states at cell level, which restricts the selection of the upper capacitor ( $C_1$ ), cell capacitor voltages of the ANPC-MMC may exhibit larger capacitor voltage ripple than HB-MMC and FC-MMC of similar rating and energy content. Although all the devices of the ANPC structure have the same voltage rating, two more IGBTs  $S_5$  and  $S_6$  are required, resulting in higher capital cost. Hence, they are not preferable in the practical application, compared with the HB cells.

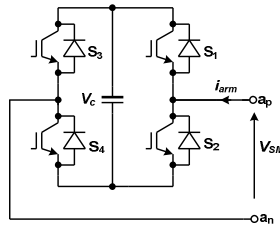
### 2.7 Mixed cells MMC (MC-MMC)

It is possible to employ a combination of different cells within an MMC, with Fig. 2 (g) depicts an example of mixed cell. A lot of combinations are theoretically possible, but most commonly referred to is a combination of half- and full-bridge cells in order to reduce semiconductor losses to less than that of the FB-MMC[35, 36], while retaining some of control flexibility of the FB-MMC such as:

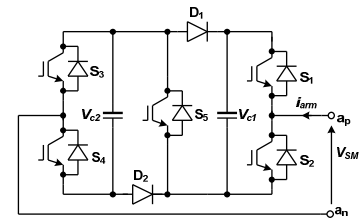
- Resiliency to dc network faults, including dc fault reverse blocking capability and controlled operation with reduced and zero dc-link voltage.
- Bipolar dc-link voltage operation can be achieved over a limited range, determined by the ratio  $\gamma = N_{FB}/N_{HB}$ ; where  $N_{FB} = N\gamma/(\gamma+1)$ ,  $N_{HB} = N/(\gamma+1)$ ,  $N$  is the total number of cells per arm ( $N = N_{FB} + N_{HB}$ ), and  $N_{FB}$  and  $N_{HB}$  are the number of full and half bridge cells per arm. This feature is necessary for arc extinction following a dc fault.
- The tributes and flexibilities in a) and b) show that the mixed cell MMC could be used to deliver customised features for a given level of semiconductor losses.



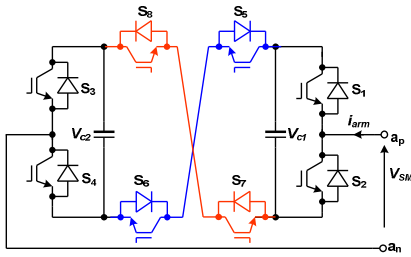
(a)



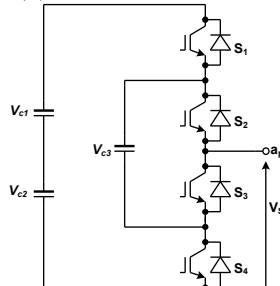
(b)



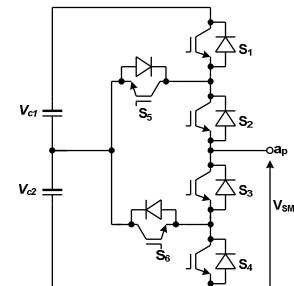
(c)



(d)



(e)



(f)

Theoretically, the MC-MMC operates using a similar principle as the FB and HB MMC and adheres to the same insertion functions described in section 2. However, its operation limits, including bipolar dc voltage operation are determined by the ratio ' $\gamma$ ' that defines the control range for ' $\alpha_d$ '. For example, when  $\gamma=1$ ,  $N_{FB}=N_{HB}=1/2N$ , which implies that the control range for dc modulation index ' $\alpha_d$ ' is:  $0 \leq \alpha_d \leq 1$ ; thus, each MC-MMC arm is able to synthesize any voltage level between  $V_{dc0}$  and  $-1/2V_{dc0}$ . Within this envelope, each MC-MMC arm can generate the necessary negative voltage to enable operation with any dc-link voltage from rated positive dc voltage ( $V_{dc0}$ ) to  $V_{dc}=0$ , without jeopardizing the converter ability to synthesize the rated ac voltage. The combination of half and full bridge cells as depicted in Fig. 2 (g) generates two positive voltage levels ( $2V_c$  and  $V_c$ ) and one negative voltage ( $-V_c$ ) and zero; therefore, it belongs to family of asymmetric cells (or simply refer to as asymmetric cell).

### 2.8 Single-clamped cell MMC (SC-MMC)

The single-clamped cell shown in Fig. 2 (h) [37] provides small negative voltage sufficiently for blocking a dc fault, exploiting additional clamp diode  $D_1$  which is connected to the mid-point of the dc capacitors  $C_1$  and  $C_2$  and middle IGBT. Compared to FB cells, the single-clamped cell requires reduced number of IGBTs, thus, leading to relatively lower capital cost. It is worth stressing that only half of the cell capacitor voltage per cell is utilized to block dc faults, and the unidirectional conduction of clamping diode  $D_1$  makes the single-clamped cell unable to generate negative voltage when the MMC under active control, resulting in restricted control range and flexibility

### 2.9 Other cell topologies

Besides the aforementioned cells, more unipolar, asymmetric and symmetric bipolar cells can be found in [37, 38]

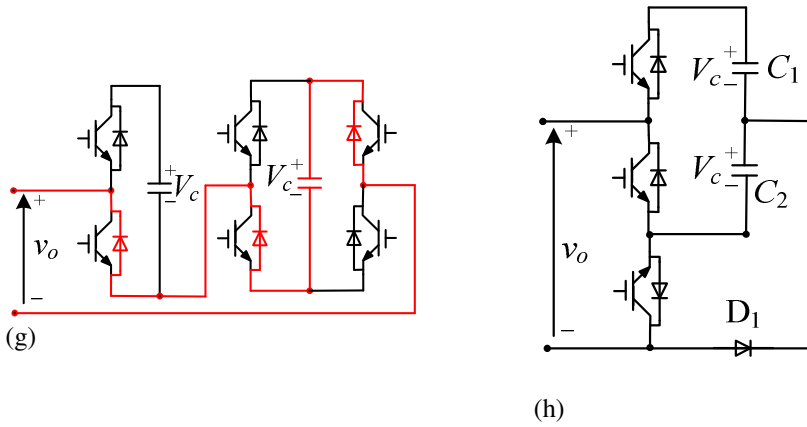


Fig. 2: Examples of MMC cells.

- (a) Half-bridge cell
- (b) Full-bridge cell
- (c) Three-level double clamped cell
- (d) Symmetrical bipolar five-level cross-connected cell
- (e) Three-level unipolar flying capacitor cell
- (f) Three-level unipolar ANPC cell
- (g) Hybrid or mixed cell
- (h) Single clamped cell

### 3. SPECIAL MULTILEVEL AC-DC CONVERTERS

Fig. 3 shows the phase legs of some common modular and hybrid multilevel converters. The following subsections discuss the attributes and shortcomings of these converters, and potential relevance to smart transmission systems.

#### 3.1 Alternative arm converter (AAC)

Fig. 3(a) shows the alternative arm converter proposed in [39, 40], which aims to reduce semiconductor losses and converter footprint (size and weight by reducing the number of cells per arm) compared to the FB-MMC, while retaining some of the attributes of the FB-MMC, such as dc fault reverse voltage blocking ability and reduced dc-link voltage operation. However, in retaining these attributes, the FB cells in each arm of the AAC must be able to block a dc voltage greater than  $\frac{1}{2}V_{dc}$ , as originally envisaged ( $\sum_{j=1}^N V_{ej}^{FB} > \frac{1}{2}V_{dc}$ ). Unlike MMC type

converters with concurrent conduction in the upper and lower arms of the same phase leg, each arm of the AAC conducts for  $180^\circ$  with the director switch in each arm used to commutate currents between arms and ensure that each arm is able to block the full dc-link voltage ( $V_{dc}$ ). With the aid of a brief overlap period at the '0' voltage level, where both upper and lower arms of the AAC conduct simultaneously, the director switch of each arm is used to facilitate current commutation between the upper and lower arms. Thus, seamless current commutation is achievable for a limited range of power factors, and beyond which large inrush current occurs in the AAC arms. Its input dc-link capacitors may increase the peak of dc fault current transient component [41].

In an effort to address the aforementioned problems and ensure satisfactory operation over full modulation index linear range and all power factors, extended overlap operation of AAC was proposed [42].

In summary, this discussion shows that the AAC is inferior to MC-MMC in terms of performance, flexibility and control.

#### 3.2 Hybrid cascaded two-level converter (HC2LC)

Fig. 3 (b) presents the hybrid cascaded two-level converter which uses a two-level converter as the main power stage that manipulates the phase and magnitude of fundamental voltage of the switched voltage ( $V_{T0}$ ) to control the converter output active and reactive powers[43]. The ac-side cascaded FB chain link of each phase operates as a series active power filter (wave shaping circuit) to inject the necessary voltage harmonics ( $V_{FB}$ ) to cancel the inherent harmonics in the switched output voltage of the two-level converter stage ( $V_{T0}$ ), thus a pure sinusoidal output voltage ( $v_{ao}$ ) is generated at output pole 'a<sub>o</sub>' relative to dc-link mid-point 'o'. If the orthogonality relationship between  $v_{FB}$  and  $i_{ao}$  is maintained, the linear range for modulation index control of the HC2LC can be extended to 1.27 without compromise to cell capacitor voltage balancing. This means the  $P$ - $Q$  envelope of the HC2LC will be larger than all MMC type converters. In the case of reactive power applications, the modulation index control range can be extended further, to 2. The HC2LC is expected to be smaller than all MMC type converters as the number of cell capacitors required per phase, is a quarter that of the HB and FB MMC. The main shortcomings of the HC2LC are[44]:

- DC fault reverse blocking capability if achieved at the expense of high semiconductor losses as the number of devices in the conduction path, carrying full load current, is higher than the AAC and MC-MMC.
- Its input dc-link capacitors contribute substantial discharge current into a dc fault, and this increases the current stresses on the dc switchgear connected to its positive and negative dc poles.
- Ensuring synchronization between the switching of the two-level converter and the chain link is challenging, and it may expose the converter transformer to high-voltage spikes of  $\pm 2V_{dc}$  in the worst-case, and with period corresponding to miss-synchronization period. These spikes tend to introduce low-order harmonics into the baseband and need filtering using ac tuned filters.
- Its operation is limited to positive dc-link voltages, and reduced dc voltage operation is possible should the



number of FB cells in the chain link be increased to be able to synthesize the nominal terminal ac voltage when the dc-link is suppressed to zero; thus, operating as a typical cascaded multilevel converter.

### 3.3 Hybrid cascaded modular multilevel converter (HC-MMC)

Fig. 3 (c) displays one-phase-leg of a hybrid converter that employs a HB-MMC in the main stage (instead of a two-level converter as in the HC2LC described in subsection 3.2) to control the fundamental voltage and power exchange between the converter ac and dc sides [45]. The operation of the ac-side FB chain link of each phase leg is as explained for the HC2LC. The low  $dv/dt$  of the staircase multilevel voltage waveform ' $V_{To}$ ' at its terminal means switching synchronization to the FB chain link involves a maximum voltage error of one cell capacitor voltage. The HB-MMC in the main stage allows the FB chain links of the HC-MMC to be used as ac circuit breakers, while the cell capacitors of the HB-MMC facilitate controlled recharge of the dc-link following dc fault clearance [45]. The HC-MMC has a large footprint, high semiconductor losses, and high cost due to its larger semiconductor area and large number of capacitors.

### 3.4 Line commutated converter with ac-side cascaded full-bridge chain link (LCC-ACFBCL)

Fig. 3 (d) shows a phase-leg of a line commutating converter that uses cascaded FB cells in its ac side as a series active power filter to ensure that the LCC stage receives a distortion free (or pure sinusoidal) commutation voltage, independent of the system operating condition at the point of common coupling[46]. Thus LCC commutation failure is avoided [46], and the entire LCC reactive power needs can be provided by manipulating the magnitude of the commutation voltage ( $v_{To}$ ) relative to the magnitude of the grid voltage ( $v_{ao}$ ) at the point of common coupling. A limited number of tuned ac filters are needed to attenuate the characteristic harmonic currents injected by the LCC stage. The main attributes and limitations of the LCC-FBCL are:

- Lower semiconductor loss than hybrid counterparts such as the HC2LC and HC-MMC.
- Increased the power handling of LCC type HVDC links, without extra equipment dedicated for provision of reactive power support.
- LCC limitations related to power flow direction and reversal remain.

### 3.5 Hybrid converter with half-bridge cells across the dc-link

Fig. 3 (e) shows a three-phase hybrid converter with three limbs of cascaded half-bridge cells connected across the dc link (one limb per phase)[47]. Each limb comprises of  $N$  half-bridge cells, supports  $1/2V_{dc}$  (where  $V_{dc}$  is the dc link voltage) and presents a rectified dc voltage ( $V_{d1}=1/2V_{dc}|\sin(\omega t+\theta)|$ ) at the input dc terminals of the high-voltage full-bridge cell of each phase that synthesises an output ac voltage such as ( $v_{a1}$ ) to be imposed on each isolated winding of the interfacing transformer (thus, switching devices of the high-voltage full-bridge cell must be rated for  $1/2V_{dc}$ ). At each instant, ' $2N$ ' half-bridge cells are selected from the ' $3N$ ' available cells in the three limbs of the three-phase converter to be used to synthesize rectified dc voltages  $V_{d1}$ ,  $V_{d2}$  and  $V_{d3}$  to be presented at dc terminals of the high-voltage full-bridge cell of each

phase-leg. The high-voltage full-bridge cell connected to output circuit of each phase-leg exploits its bi-polar switching capability to generate positive and negative halves of the output phase voltages (such as  $v_{a1}$  for phase 'a') from the rectified dc voltages (such as  $V_{d1}$  for phase 'a') being presented by the cascaded half-bridge cells of the three limbs. To avoid uncontrolled inrush current, the half-bridge cells to be inserted into the power path at each instant must be selected all three limbs and must be sufficient to match the input dc link voltage ( $V_{dc}$ ), i.e.,  $V_{d1}+V_{d2}+V_{d3}\approx V_{dc}$ . Thus, a large dc inductor ( $L_{dc}$ ) is needed in the dc link in order to suppress any potential inrush current that may arise due to any voltage mismatch between ( $V_{d1}+V_{d2}+V_{d3}$ ) and the input dc link voltage ( $V_{dc}$ ). This constraint makes the hybrid converter in Fig. 3 (e) unable to generate an ac voltage with variability magnitude, and this is the main weakness of this hybrid converter.

### 3.6 Other hybrid multilevel converters

The authors in [48, 49] proposed a controlled transition bridge (CTB) converter that avoids high  $dv/dt$  and excessive switching losses of the conventional two-level converter by employing FB chain-links rated for half of the dc voltage ( $V_{dc}$ ) and trapezoidal type modulation to facilitate stepped transitions of the output voltage between two extrema of  $+1/2V_{dc}$  and  $-1/2V_{dc}$ , with each voltage step is defined by the voltage of one cell capacitor of the FB chain-link. The director switches of CTB converter experience slow and gradual build-up of the voltage and switch at zero voltage; director switches do not require stringent series connection of IGBTs and incur zero switching losses. But trapezoidal modulation imposes limited control range and high ac side filtering. Extensive discussions of sinusoidal operation of CTB proposed in [50, 51] show that it generates high quality multilevel ac voltage as MMCs, and requires large dc side filtering which increases dc fault level.

Reference [52] has proposed a hybrid multilevel converter that represents a modified version of an AAC, but with the node between the director switch ( $S_{D1}$  or  $S_{D2}$ ) and cascaded half or full bridge chain-link of each arm is clamped to ground (O) through additional director switch ( $S_{C1}$  or  $S_{C2}$ ), see Fig. 3 (f). The chain-links of upper and arms of each phase leg are utilized to shape the output ac voltage ( $v_{ao}$ ), with the director switches operate alternately every half fundamental cycle. It has been claimed in [52] that the proposed converter requires fewer cells and reduced energy storage requirement over full power factor range. As in an AAC, its director switches operate at zero voltage switching, hence, leading to reduced switching losses. However, the director switches of the proposed converter must be designed to withstand voltage stresses amount to half of the rated DC voltage; thus, a large number of series-connected IGBTs are required.

In [53] an improved alternate arm converter (IAAC) was presented, in which the director switches of each phase leg are realized by flying capacitor cell. The proposed IAAC addresses the problem of current commutation between the arms and eliminate the dependency on power factor and modulation depth, and no sizable input capacitors or inductors are required for filtering as in conventional AAC.

In [54, 55] a compact mixed cell modular multilevel converter which is created by realizing the director switch in each arm of conventional AAC by high-voltage half-bridge cell is proposed. The proposed CMC-MMC offers all the attributes of conventional MC-MMC described earlier.

Recently, an hybrid converter based on active forced commutated bridge (AFC-B) is proposed for UHVDC transmission systems with rated powers and voltages up to 3000MW and 800kV per converter[55, 56]. The proposed hybrid converter requires large ac and dc side filtering, and apart from that it offers many of the features of the FB-MMC at reduced semiconductor losses, thanks to the use of symmetrical thyristors in the main conduction paths. Moreover, it employs the FB chain-links in its limbs to actively commutate the current between the upper and lower arms of the same phase-leg; with no risk of commutation failure. The proposed converter can block dc fault, operate with positive and negative dc voltages, reverse active power with change of

polarity of dc current or voltage polarity, generate leading and lagging reactive powers and resilient to both ac and dc faults.

Reference [57] presented a novel hybrid converter with alternate common arm and director switches that resembles a further Improvement to the AFC-B converter in [55, 56]. The presented converter uses thyristors in alternate arms that operate as director switches, and FB chain-link in common arm and in the upper and lower arms similar to that of the conventional FB-MMC. In this way, it nearly doubles the current capability of each arm, hence, the power rating, while retaining the power quality of the ac and dc sides as that of the MMCs.

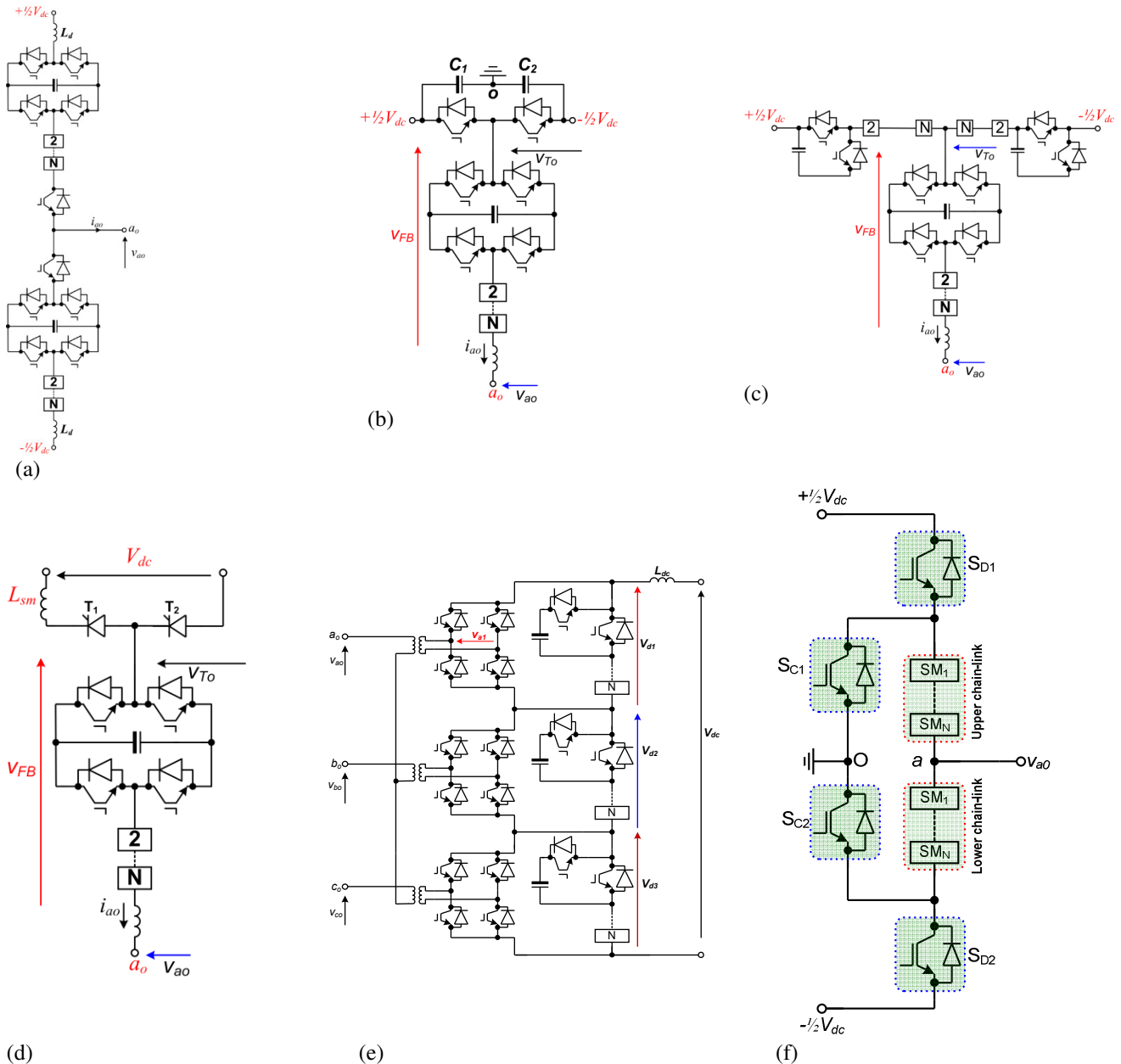


Fig. 3: Examples of converter (leg) topologies for HVDC transmission systems

- (a) Phase-leg of alternative arm converter
- (b) Hybrid cascaded two-level converter
- (c) Hybrid cascaded modular multilevel converter
- (d) Hybrid converter with LCC and ac-side cascaded FB cells
- (e) Hybrid converter with half-bridge cells across the dc-link
- (f) Hybrid multilevel converter with SMs connected to AC terminal (HMC-AC)

## 4. DC-DC CONVERTERS

Fig 4. shows examples of dc-dc converter topologies with potential to be applied in large-scale HVDC transmission networks to perform voltage matching or tapping, and can act as flexible dc controllers to regulate power in highly meshed dc networks [58].

### 4.1 Front-to-front dc-dc converter topology

The front-to-front (F2F) dc-dc converter is described in [59-64]. The converter terminals VSC<sub>1</sub> and VSC<sub>2</sub> can employ any of the converter topologies summarised in Fig. 1 and Fig. 3, with one converter acts as reference that defines the ac voltage and frequency in the internal ac-link, and other converter controls dc power or dc voltage. Although high-frequency square waveform voltage operation of VSC<sub>1</sub> and VSC<sub>2</sub> has been adopted in low and medium voltage applications for many years [59-64], sinusoidal or trapezoidal (quasi-two-level) voltage waveform in the ac-link with fundamental frequency ranging from 200Hz to 500Hz is likely to be adopted in HVDC applications, with dc operating voltages up to 800kV [58, 65-67].

Besides dc voltage matching, power regulation and dc voltage regulation, the F2F dc-dc converter decouples the dc systems as it can block dc fault propagation from the faulty system to the healthy system. Therefore, the F2F dc-dc converter is suitable for splitting large dc networks into several protection zones to contain the impact of dc fault within a well-defined zone. The main shortcomings of the F2F dc-dc converter are:

- Both converter terminals must be fully rated (1 per unit); thus, its semiconductor losses resemble that of the two-terminal HVDC link.
- Its dc voltage matching range is limited by the current stresses in the converter switches of the low-voltage side.

The isolated front-to-front dc-dc converter is shown in Fig 4(a). The provided galvanic isolation is necessary for connection of dc system with a separate dc ground.

The F2F converter can also be realised without isolation. In this case, the transformer is replaced by a simple inductor. Although a non-isolated F2F dc-dc converter in HVDC applications can reduce costs, there are major drawbacks of not having isolation. The implication of under-modulation in the non-isolated F2F dc-dc converter is that the switching devices of its high-voltage converter are subjected to the same ac currents as that of the low-voltage converter, which are higher than its isolated counterpart. Thus, high semiconductor losses are incurred in the high-voltage side.

### 4.2 Multi-pole multi-module front-to-front dc-dc converter topology

Fig. 4(b) shows a configuration that employs series-input and series output to connect a symmetrical mono-pole dc system to a symmetrical multi-pole dc system, with each sub-converter in Fig. 4 (a) realized with modular type converters, or two-level or NPC converters, with each rated at a higher dc voltage and power than in traditional medium-voltage applications. With the multipole side being limited to tri-pole, the voltage stresses on the upper and lower transformers in the ac-link could be limited to slightly higher than that of conventional bipolar HVDC link[68].

### 4.3 Partially isolated dc-dc converter topology

Fig. 4(c) shows schematic diagram of an efficient partially isolated dc-dc converter that can be used for voltage matching and tapping in dc systems with a common dc ground [69, 70]. The total dc power at the high-voltage dc terminal ( $P_{dc1}$ ) transfers to the low-voltage dc terminal ( $P_{dc2}$ ), without the need for the switching devices of any of the sub-converters to be rated for full power. The power flow between the two dc terminals of dc-dc converter topology in Fig. 4 (b) is explained, assuming the power flow is from the high to low voltage dc terminals as follows:

- The total dc power  $P_{dc2}$  splits into ac power  $P_{ac}$  and dc power  $P_{dc12}$ .
- $P_{ac}$  represents the component transferred through the ac side and it determines the magnitudes of ac and dc currents in the arms of VSC<sub>1</sub> and VSC<sub>2</sub> for a given transformer voltage ratio. This component can be approximated by:  $P_{ac} \approx (V_{dc1} - V_{dc2})I_{dc1} \approx P_{dc1}(n-1)/n$ , where  $n = V_{dc1}/V_{dc2}$ .
- $P_{dc12}$  represents the power component transferred directly to the low-voltage dc terminal using dc components of the arm currents, without passing through the switching devices of VSC<sub>2</sub>; and can be approximated by:  $P_{dc12} \approx I_{dc1}V_{dc2} \approx P_{dc1}/n$ .

In this manner, the switching devices of VSC<sub>1</sub> and VSC<sub>2</sub> must be rated to handle the current stresses corresponding to ac power of  $P_{dc1}(n-1)/n$ , and dc operating voltage of  $V_{dc1}(n-1)/n$  and  $V_{dc1}/n$  respectively.

### 4.4 Non-isolated MMC-based dc-dc converter

The converter in Fig. 4(d) is formed by series connection of two MMCs (HB or mixed cells type); however, the mixed cells approach is preferred because it blocks dc fault propagation from the faulty side to the healthy side, due its FB dc fault blocking capability [60]. Although this dc-dc converter does not use an isolation transformer, the coupling inductor being employed in the positive and negative poles of the low-voltage dc terminal must be insulated to withstand the high dc voltage stress corresponding to the dc-link voltage of the low-voltage dc terminal,  $V_{dc1}$ . Additional weakness of this topology is that the fundamental ac component being used to exchange power between converter arms needs to be filtered using large passive filters ( $L_f$  and  $C_f$ ). Based on this discussion, this non-isolated dc-dc converter topology is inferior to the partially isolated topology, as described in the previous section.

### 4.5 Full-bridge-based Non-isolated hybrid cascaded two-level dc-dc converter

Fig. 4(e) shows a full-bridge-based non-isolated hybrid cascaded two-level dc-dc converter, where the dc-link of the two-level converter stage represents the high-voltage side ( $V_{dc2} > V_{dc1}$ )[71]. The submodules of each limb at the low-voltage side must be of the full-bridge type so that it can inject the necessary bipolar ac voltage waveform to cancel some of the generated voltage by the two-level converter stage. In this way, a ripple-free fully-controlled dc voltage with magnitude  $V_{dc1}$  will be generated at the low-voltage dc terminal. This means the series connected switching devices of the two-level converter stage must be rated for high-voltage side voltage ( $V_{dc2}$ ). Inhibiting the gating signals is sufficient to prevent dc fault propagation from one side to the other, independent of the fault location (dc short circuit). Lack of isolated dc ground may require system shutdown during a pole-to-ground dc fault to prevent exposure of the healthy pole to excessive dc voltage



stresses. In this topology, the number of semiconductor devices in the conduction path (thus, conversion loss) is the same as in F2F dc-dc two-level converter, but its overall losses and semiconductor area remain lower than F2F dc-dc converter topologies.

4.6 Half-bridge-based non-isolated hybrid cascaded two-level dc-dc converter

Fig. 4(f) shows a half-bridge-based non-isolated hybrid cascaded two-level dc-dc converter, where the dc-link of the

two-level converter stage represents the low-voltage dc terminal ( $V_{dc1} > V_{dc2}$ ), and cascaded HB cells are used (instead of the FB cells) as each limb only needs to inject a unipolar voltage waveform to boost the output dc voltage[71]. In this scenario, the chain link of each limb must be able to support the full dc voltage of the high-voltage side.

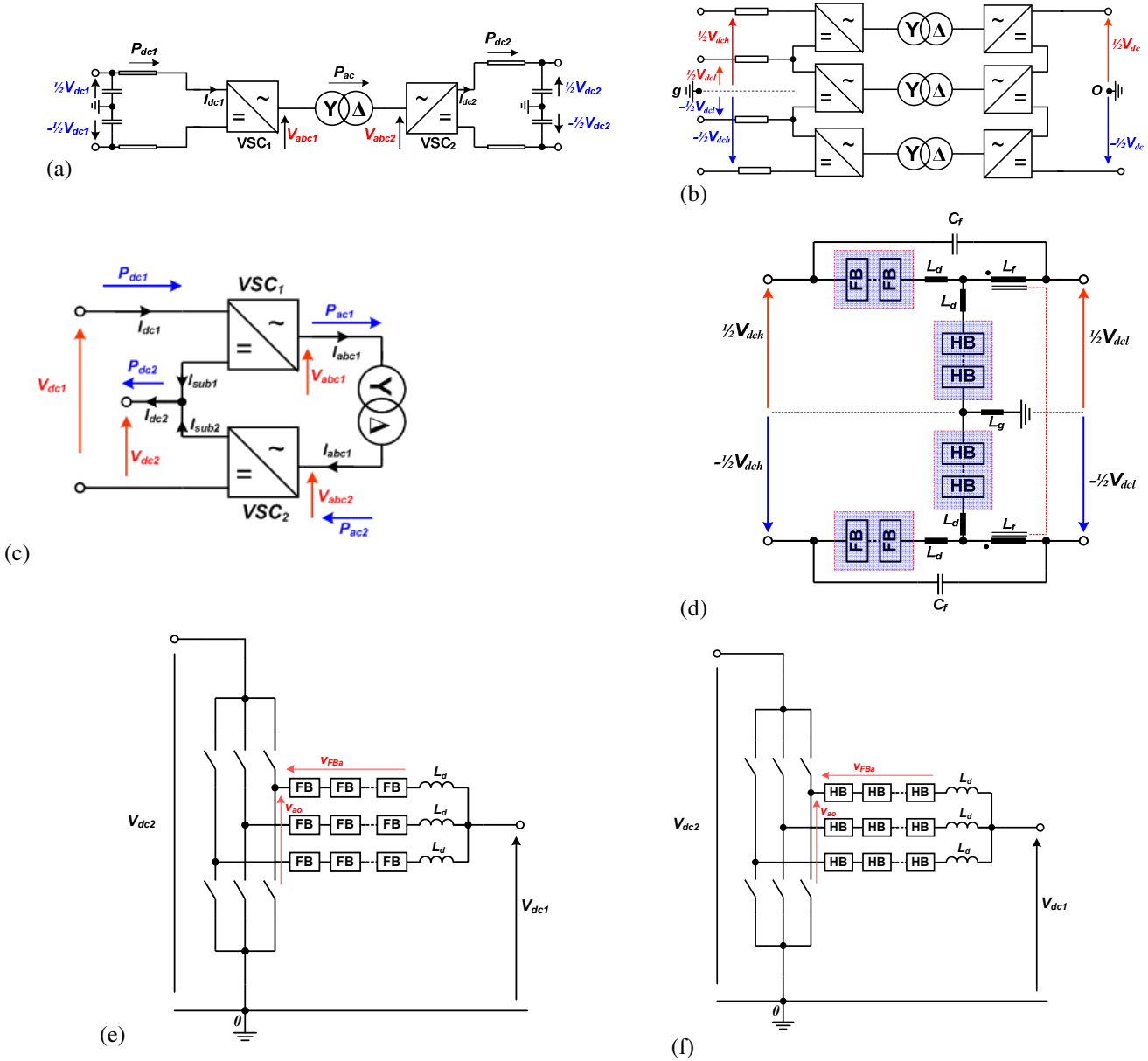


Fig. 4: Other examples of dc-dc converter topologies  
 (a) Front-to-front dc-dc converter  
 (b) Isolated front-to-front dc-dc converter with one side connected to multi-pole dc system  
 (c) Partially isolated dc-dc converter  
 (d) Non-isolated MMC based dc-dc converter  
 (e) Non-isolated hybrid cascaded two-level dc-dc converter  
 (f) Half-bridge-based non-isolated hybrid cascaded two-level dc-dc converter

## 5. SERIES-TYPE DC FLOW CONTROLLING DEVICES

Besides dc fault ride-through challenges highlighted in previous sections, full utilization of dc lines in meshed multi-terminal HVDC transmission networks that contain a number of floating dc nodes is extremely important for efficient operation of dc grid. However, control of the dc power flows on the individual dc lines that form a mesh is technically challenging [72] as the current split between parallel paths is solely determined by the Ohm and Kirchoff laws. Unlike in an ac system, a dc system does not have a phase angle or reactive power, giving less degree of freedom to control the power flow. To realise better utilization of dc cables in a meshed MT-HVDC network, the dc equivalent of the FACTS devices, such as power shifters, are beneficial to optimize the power flow within the dc network.

This task can be performed by incorporating appropriate dc/dc converters or interline series type current controlling devices [73-75]. Although series type power controlling devices appear effective and cost effective, their ability to survive dc short circuit faults are yet to be demonstrated. Apart from isolating transformers, all the power electronic parts are fractionally rated. In addition to dc-dc converter discussed in section (e), some of the proposed methods for power flow control in MT-HVDC networks are discussed briefly in the following subsections

### 5.1 Controlled Series Resistor

Fig. 5(a) show a dc power controller that uses a series switched resistor to regulate the power flow between two dc nodes by manipulating the dc voltage drop of the line that connects these dc nodes[73-75]. Although this solution seems to be simple and effective, it has a limited control range.

### 5.2 Series Current Flow Controllers

Amongst several series current flow controllers proposed in [74, 76-80], Fig. 5(b) and (c) show examples of series connected bi-directional dc current or power flow controllers capable of controlling power flow in individual dc lines by inserting small positive or negative dc voltage in series with a given dc line, depending on the power flow direction [74, 78-80]. These power flow controllers incur low on-state losses as they present small number of semiconductor devices in conduction path. Extensive studies performed in [74, 78-80] show these series controllers are able to operate satisfactorily over wide range of operating conditions and can survive dc faults.

### 5.3 Series Voltage Injection

The solution in Fig. 5(d) can control dc power in a given dc line from zero to the rated power and in a reverse direction due to its ability to inject positive or negative dc voltage in series with the line [73-75]. This device is equivalent to a unified power flow controller in an ac system.

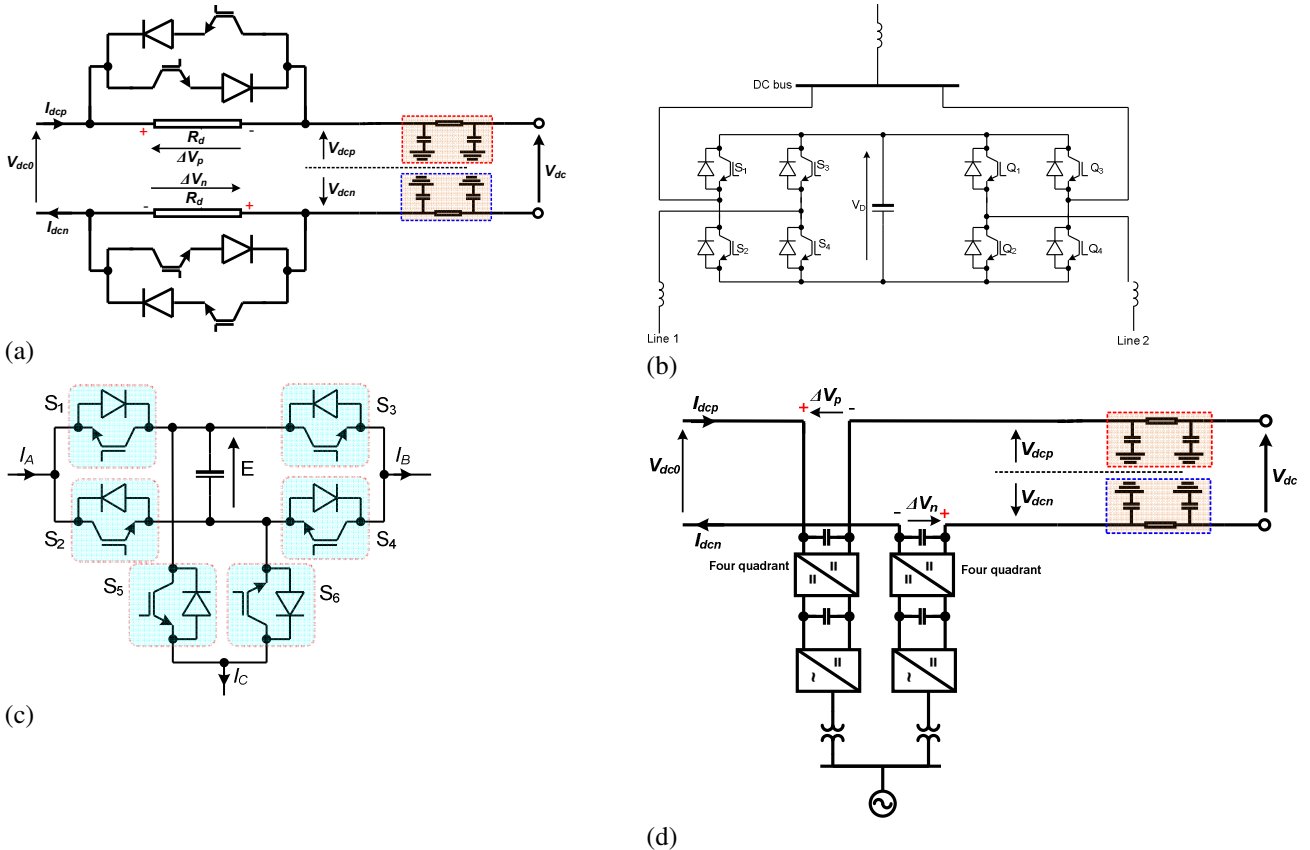


Fig. 5: (a) and (b) are examples fractionally rated dc series power controller for highly meshed multi-terminal HVDC network

## 6. DC CIRCUIT BREAKERS

The current absence of a cost-effective high-voltage dc circuit breaker (DCCB) is the main missing element prevent

bringing dc grids in line with ac counterpart. Its absence denies the ability to isolate the faulty dc part while allowing the remaining healthy parts of the dc grid to operate normally. Being able to continuously exchange power is paramount from

a supply reliability and security point of view. Although the technology for solid-state dc circuit breakers has existed since the 1990s and is improving, they incur excessive semiconductor losses and cost [81-89]. Fig. 6 and Fig. 7 summarise some of the main dc circuit breakers being suggested for dc fault current interruption in multi-terminal dc networks, targeting different fault clearance times.

### 6.1 Hybrid DC Circuit Breakers

Fig. 6(a) and (b) show types '1' and '2' hybrid dc circuit breakers that exploit a voltage injection method to force the fault current to zero, where the injected dc voltage must be larger and oppose that being presented by the faulty line [81, 88, 89]. During normal operation, the main conduction path for the dc current is through a low-voltage rated semiconductor switch known as a load commutation switch (LCS) and low-resistance mechanical ultra-fast disconnecter (UFD) with SF6 as insulation media and a 2ms opening time. The mechanical UFD must be designed to support the prospective dc voltage when opened. When the dc fault is detected in the type '1' DCCB, the LCS is turned off to initiate commutation of the dc fault current from the principle conduction path to the main circuit breaker (MCB), which is a typical high-voltage semiconductor switch, capable of carrying high current for

short period (<10ms) [90, 91]. After the entire dc fault current is commutated to the MCB, the mechanical UFD is opened at near zero current and voltage, and during this period the fault current continues to flow in the MCB, and then, the MCB is opened to interrupt the dc fault current. More details on Fig. 6(a) are presented in [88, 89].

The type '2' DCCB in Fig. 6(b) turns off LCS when a dc fault is detected and triggers the switching delay branches in a progressive manner in order to commutate the fault current from the main conduction path to the arming branch. The current in each switching delay branch drops to zero when its capacitor charges to the blocking voltage across the LCS. After the entire fault current is transferred to the arming branch and all thyristors of the switching delay branches are off and carry zero current, the mechanical UFD is turned off. This is followed by gating-off the composite thyristor of the arming branch to interrupt the fault current to force the surge arrester across the arming branch to absorb the entire inductive energy of the faulty line and to force the fault current to zero [81]. The hybrid dc circuit breakers in Fig. 6(a) and (b) are intended for faster current interruption, ranging from 3ms to 5ms.

The hybrid DCCB in Fig. 6(c) and (d) [87, 92] have similar on-state losses and operating speed as the counterparts in Fig. 6 (a) and (b).

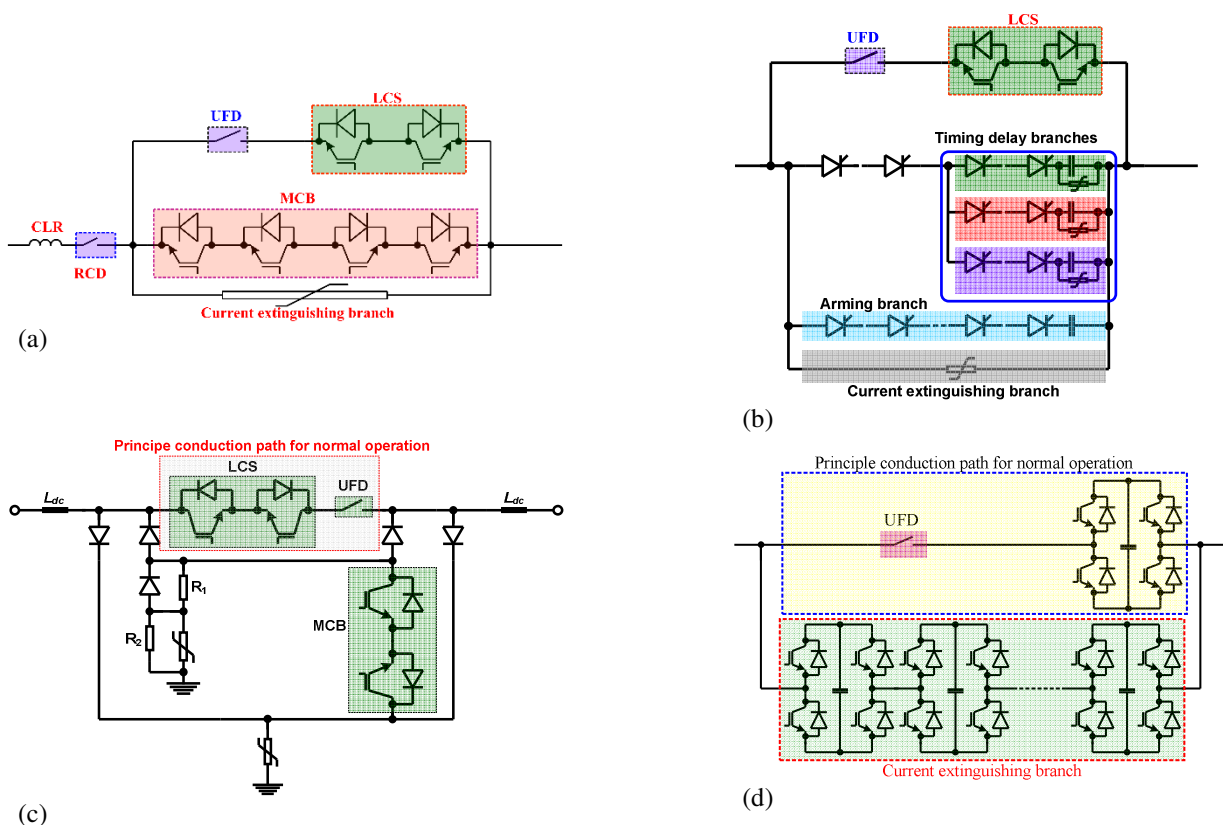


Fig. 6: Some hybrid dc circuit breakers being proposed for use for dc fault isolation in dc grids

- (a) Type 1 hybrid dc circuit breaker
- (b) Type 2 hybrid circuit breaker
- (c) Type 3 hybrid dc circuit breaker

Type 4 hybrid dc circuit breaker

### 6.2 Resonant DC Circuit Breakers

Fig. 7 (a) shows a forced current zero resonance dc circuit breaker that uses a pre-charge capacitor to initiate resonance with the aim of creating a speedy current zero when the

negative peak of the resonant current component larger than the dc component of the fault current [85]. In [85], this approach interrupts a dc fault current up to 21kA, within 8ms to 10ms.

Fig. 7 (b) and (c) show other versions of low-loss active resonance based dc circuit breakers [84]. The versions of the active resonance DCCBs displayed in Fig. 7 (b) and (c) are expected to have similar performance (on-state loss, current breaking capability and operating speed) as that presented in Fig. 7 (a), where the options in Fig. 7 (a) and (b) permit easy incorporation of additional resonance branches that facilitate execution of several successive fault clearance attempts.

Besides relatively slow resonant DC circuit breakers discussed above, reference [93] presented a cost effective fast acting resonant based hybrid DC circuit breakers that uses vacuum AC circuit breaker technology in parallel with resonance branch that uses half-bridge or full-bridge cells to initiate high frequency resonance, see Fig. 7 (d). Each

resonance branch consists of HB or FB cell in series with inductor and capacitor, and when the fault is detected the HB or FB cell will be switched at 10kHz to impose bipolar square waveform voltage in each resonance branch, causing high frequency bipolar oscillating current with increasing magnitude to be superimposed on the DC fault current. Operation of HB or FB cell at each resonance branch at 10kHz permits creation of multiple current zeros within 1ms (recall that the current zeros are created when the negative peaks of the oscillating current equal or exceed the magnitude of the actual DC fault current). In this manner, the DC circuit breaker in [93] is able to interrupt DC faults within sub-milliseconds, provided that the protection systems responsible for fault discrimination is able to operate with such speed.

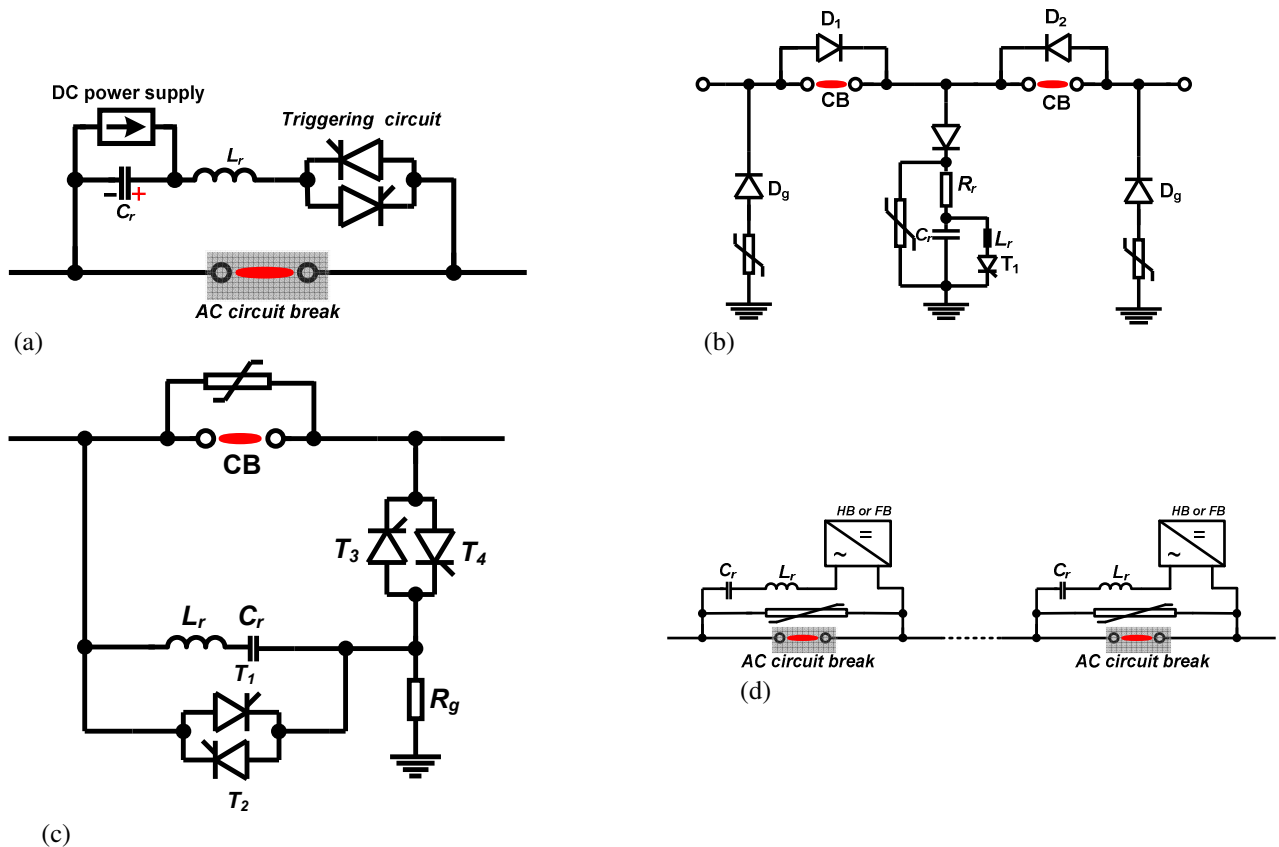


Fig. 7: Some resonant dc circuit breakers being proposed for use for dc fault isolation in dc grids

- (a) Forced current zero resonance circuit breaker (type 1)
- (b) Forced current zero resonance circuit breaker (type 2)
- (c) Forced current zero resonance circuit breaker (type 3)
- (d) Forced current zero resonance DC circuit breaker (type 4)

## 7. DISCUSSIONS

Based on critical review of the open literature, the main findings of this work are highlighted as follows:

1) **Modular multilevel converters:** It is established that the MMCs with asymmetrical and symmetrical bipolar cells can block and control dc fault current, and remain controllable for a wide range of dc voltages, and these features are useful for pole restraining during pole-to-ground dc fault. Therefore, MC-MMC as a representative of the MMCs with asymmetric bipolar cells offers all flexibilities needed for efficient, reliable and fault-tolerant operation of VSC based dc grids. Nonetheless, extra control range offered by the MMCs with symmetrical

bipolar cells such as the FB-MMC are well-suited for generic dc grids that employ both VSCs and LCCs (thanks to the ability to operate with positive and negative dc voltages, and reverse power flow direction by change of dc current or voltage polarities).

2) **Hybrid multilevel converters:** Section 3 establishes that the AFC-B converter and hybrid converter with alternate common arm and director switches in [55-57] offer most of the features of the FB-MMC at much lower semiconductor losses. The former increases the power capability at reduced semiconductor losses but requires substantial ac and dc filtering. Whilst the latter increases

- the power capability with no filtering requirements at ac and dc sides, thanks to additional current path provided by the thyristor based director switches which conduct alternately, i.e., upper director switch conducts for half fundamental cycle with the upper arm of the FB-MMC and vice versa. The latter hybrid converter resolves the current commutation problem of the conventional AAC and its variants [39, 40, 42, 53, 54, 94, 95]. These hybrid converters are well-suited for generic and large dc grids, where the LCCs are expected to operate alongside VSCs. On other hand, hybrid converters in [53, 54] are viable alternative to conventional AAC and MC-MMC and most of the MMCs with asymmetric bipolar cells, particularly in applications with confined space as they offer all features of MC-MMC with arguably reduced footprint and power circuit and control complexity.
- 3) **DC-DC converters:** Isolated F2F dc-dc converters offer many desirable features for reliable operation of dc grids such as prevention of dc fault propagation and pole shifting in the healthy side during pole-to-pole and pole-to-ground dc faults respectively, and dc voltage matching and power control (it worth stressing that these features are essential for partial selective dc grid protection strategies that employ the zoning concept). However, high capital cost and semiconductor losses may hinder their acceptance as economic solution. Non-isolated F2F dc-dc converters are unable to prevent pole-shifting during pole-to-ground dc fault and suffer from high losses and poor utilization of the semiconductor of the high-voltage converter, therefore, not viable for dc grids. Partially isolated dc-dc converter in [69, 70, 96] is attractive economically as it permits the transformer in its ac link and sub-converters to be fractionally rated. Its multi-port version that generates multiple and independent dc and ac voltages is attractive for complex hub that facilitates dc and ac voltage tapping and matching and power control, with bespoke ability to precisely define the route of the power flow from a given input to a given output[96, 97]. The non-isolated MMC and hybrid cascaded two-level dc-dc converters in [71, 98] offer cost-effective solution for dc voltage matching between two dc systems with common ground.
- 4) **Series current flow controllers:** Fractionally rated bidirectional interline current or power flow controllers in [74, 76-80] offer low cost solutions for controlling and rerouting dc currents or dc powers within the dc grids away from the bottlenecks and over-loaded dc cables; thus, these devices are expected to play major roles in large dc grids that include floating dc nodes.
- 5) **DC circuit breakers:** Section 6 reviews a number of basic dc circuit breaker technologies, covering fault isolation time-scales ranging from 2ms to 15ms. It is found that although the hybrid dc circuit breakers offer faster fault clearance times (2ms to 5ms) which is critical for continued operation of dc grids, their large semiconductor areas make them expensive and vulnerable to rapid rise of fault current, particularly, in large dc grids that operate at dc voltages above 640kV and contain a number of long dc cables. Resonance based mechanical dc circuit breakers offer slower fault clearance time (up to 15ms) and require large dc inductances to be installed strategically across the dc grid to slowdown the rate of rise of fault currents and fault propagation through the dc grid. Nevertheless, mechanical dc circuit breakers remain practically attractive because of their relatively low cost and small semiconductor areas, primarily, in the resonant branch. Active resonance dc circuit breaker with reduced semiconductor area proposed in [93] offers the best overall trade-offs between performance (fault clearance times in order of 3ms to 5ms) and cost. However, an economic mechanism for sustaining the dc voltage of the fractionally resonant as soon as dc fault is detected remains to be solved. The concept of multiline dc circuit breaker proposed in [99, 100] represents an economic way to protect multiple dc cables connected to a single dc node using one current breaking branch. In this way, the overall cost of the dc grid protection can be reduced substantially. In summary, Table 7-1 to Table 7-5 provide high-level summary of the main aspects discussed earlier.

Table 7-1: High-level comparison MMCs the employ unipolar cells, and asymmetric and symmetric bipolar cells [42, 50, 53, 54, 101-112], where P and Q stand for active and reactive powers,  $V_{dc}$  is the dc voltage, and  $V_{dc0}$  stands for rated dc voltage.

	MMC with unipolar cells	MMC with asymmetric bipolar cells	MMC with symmetric bipolar cells
DC fault blocking	No	Yes	Yes
Control of fault current	No, therefore, necessitates the use of fast acting dc circuit breakers plus large dc inductors to quickly isolate dc faults and prevent over-stressing of the converters' semiconductor switches.	Yes, therefore, a range of options available, ranging from relatively cheap mechanical dc circuit breakers to simple ultra-fast dc switches could be combined with fault current capability of the MMCs with asymmetric bipolar cells to isolate dc faults.	Yes, therefore, a range of options available, ranging from relatively cheap mechanical dc circuit breakers to simple ultra-fast dc switches could be combined with fault current capability of the MMCs with symmetric bipolar cells to isolate dc faults.
Active and reactive power	<ul style="list-style-type: none"> <li>a) Independent control of P and Q, with maximum capacitive Q is limited by dc voltage limit and inductive Q by current limit.</li> <li>b) P reversal is achieved by change direction of <math>I_{dc}</math>, while <math>V_{dc}</math> remains positive.</li> <li>c) Losses control over P and Q when the <math>V_{dc}</math> falls below line-to-line voltage at converter ac side</li> </ul>	<ul style="list-style-type: none"> <li>a) Independent control of P and Q, with maximum capacitive Q is limited by dc voltage limit and inductive Q by current limit.</li> <li>b) P reversal is achieved by change direction of <math>I_{dc}</math>, while <math>V_{dc}</math> polarity remains positive.</li> <li>c) Retains control over P and Q for wide range of positive dc voltage, <math>0 \leq V_{dc} \leq V_{dc0}</math>; where <math>V_{dc0}</math> is the rated dc voltage.</li> </ul>	<ul style="list-style-type: none"> <li>a) Independent control of P and Q, with maximum capacitive Q is limited by dc voltage limit and inductive Q but current limit. However, maximum capacitive reactive power can be extended if over-modulation capability is exploited.</li> <li>b) P reversal can be achieved by change the polarities of <math>I_{dc}</math> or <math>V_{dc}</math>.</li> <li>c) Retains control over P and Q for very wide range of dc voltage, <math>-V_{dc0} \leq V_{dc} \leq V_{dc0}</math>.</li> </ul>

DC voltage polarity and range	Remain controllable for narrow range of positive dc voltages which are greater than the peak of the line-to-line voltages the interfacing transformers impose at MMCs ac terminals. Therefore, MMCs with unipolar cells only applicable to VSC based dc grids.	Remain controllable for wide range of positive dc voltages, $0 \leq V_{dc} \leq V_{dc0}$ . Therefore, MMCs with asymmetric bipolar cells applicable to VSC dc grids, and hybrid dc grids with combinations of VSCs and LCCs provided that unidirectional power flows are contemplated in all LCC terminals.	Remain controllable for very wide range of positive and negative dc voltages, $-V_{dc0} \leq V_{dc} \leq V_{dc0}$ . This feature permits operation in generic dc grids alongside LCCs, without compromising bidirectional power flow at LCC terminals.
Internal fault management	Yes, and realized by bypassing of faulty cells; hence, simpler cell structures such as HB are preferred for ease of identification of the faulty cells.	Yes, and realized by bypassing of faulty cells; hence, simpler cell structures such as HB and FB are preferred for ease of identification of faulty cells.	Yes, and it is realized by bypassing of faulty cells; hence, simpler cell structures such as FB are preferred for ease of identification of faulty cells. Five-level cross-connected cell is an alternative for FB cell that delivers MMC with similar features as FB-MMC, but its complex structure increases the complexity of internal fault management.
Over-modulation	No, even though the MMCs with unipolar cells include redundant cells to facilitate continued operation during internal faults, these cells remain unusable for extension of modulation index linear beyond 1.155; this limit is due to single polarity of the voltages that the unipolar cells generate.	Yes, should the MMCs with asymmetric bipolar cells include redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the maximum achievable ac voltage, exploiting limited bipolar capability of the asymmetric bipolar cells.	Yes, should the MMCs with asymmetric bipolar cells include redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage, exploiting full bipolar capability of the symmetric bipolar cells.
Semiconductor losses	low	medium	high

Table 7-2: High-level comparison selected hybrid converters (A≡ AAC, B≡ CMC-MMC, C≡ AFC-B converter, and D≡ hybrid converter with alternate common arm and director switches)[42, 54-57, 95, 113-119]

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
DC fault blocking	Yes,	Yes	Yes	Yes
Resiliency to ac faults	Resilient to symmetrical ac fault, but unsatisfactory performances during severe unbalanced ac grids and asymmetrical ac faults.	Yes, resilient to symmetrical and asymmetrical ac faults.	Yes, resilient to symmetrical and asymmetrical ac faults.	Yes, resilient to symmetrical and asymmetrical ac faults.
control of fault current	Yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical dc circuit breakers to simple ultra-fast dc switches could be used to ride-through dc faults.	Yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical dc circuit breakers to simple ultra-fast dc switches could be used to ride-through dc faults.	Yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical dc circuit breakers to simple ultra-fast dc switches could be used to ride-through dc.	Yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical dc circuit breakers to simple ultra-fast dc switches could be used to ride-through dc faults, including fault clearance.
Active and reactive power control	a) Independent control of P and Q, but with very limited reactive power. b) P reversal is achieved by change polarity of $I_{dc}$ , while $V_{dc}$ polarity remains positive. c) Retains control over P and Q for wide range of positive dc voltage, $0 \leq V_{dc} \leq V_{dc0}$ .	a) Independent control of P and Q b) P reversal is achieved by change polarity of $I_{dc}$ , while $V_{dc}$ polarity remains positive. c) Retains control over P and Q for wide range of positive dc voltage, $0 \leq V_{dc} \leq V_{dc0}$	a) Independent control of P and Q. b) P reversal is achieved by change of polarities of $I_{dc}$ or $V_{dc}$ . c) Retains control over P and Q for very wide range of positive and negative dc voltages, $-V_{dc0} \leq V_{dc} \leq V_{dc0}$ .	a) Independent control of P and Q. b) P reversal is achieved by change of polarities of $I_{dc}$ or $V_{dc}$ . c) Retains control over P and Q for very wide range of positive and negative dc voltages, $-V_{dc0} \leq V_{dc} \leq V_{dc0}$ .
DC voltage polarity and control range	Remain controllable for wide range of positive dc voltages, $0 \leq V_{dc} \leq V_{dc0}$ . Despite the above features, compatibility of AAC with other VSC topologies such as MMC in dc grids, and hybrid dc grids with combinations of VSCs and LCCs remain debatable.	Remain controllable for wide range of positive dc voltages, $0 \leq V_{dc} \leq V_{dc0}$ . Therefore, CMC-MMC is applicable to VSC based dc grids, and hybrid dc grids with combinations of VSCs and LCCs provided that the unidirectional power flows are contemplated in all LCC terminals.	Remain controllable for very wide range of positive and negative dc voltages, $-V_{dc0} \leq V_{dc} \leq V_{dc0}$ . This feature permits operation in generic dc grids alongside LCCs, without compromising bidirectional power flow at LCC terminals.	Remain controllable for very wide range of positive and negative dc voltages, $-V_{dc0} \leq V_{dc} \leq V_{dc0}$ . This feature permits operation in generic dc grids alongside LCCs, without compromising bidirectional power flow at LCC terminals.
Internal fault management	Yes, faulty cells of the FB chain-links are bypassed; while the director switches necessitate the use of press-pack IGBTs or IGBTs with fail safe short circuit mode. Thus, redundant cells and	Yes, faulty cells of the FB chain-links are bypassed; while the director switches necessitate the use of press-pack IGBT with fail safe short circuit mode. Thus, redundant cells and press-	Yes, faulty cells of the FB chain-links are bypassed; while the director switches necessitate the use of symmetrical thyristors that fail in safe short circuit mode. Thus, redundant cells	Yes, faulty cells of the FB chain-links are bypassed; while the director switches necessitate the use of symmetrical thyristors that fail in safe short circuit mode. Thus, redundant cells



	press-pack IGBTs must be incorporated in the FB chain-links and director switches respectively.	pack IGBTs must be incorporated in the FB chain-links and director switches respectively.	and thyristors must be incorporated in the FB chain-links and director switches respectively.	and thyristors must be incorporated in the FB chain-links and director switches respectively.
Over-modulation	Yes, should the AAC contains redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage.	Yes, should the CMC-MMC contains redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage.	Yes, but limited to maximum modulation index of 1.27; thus, the magnitude of the maximum achievable ac voltage.	Yes, should the hybrid converter with alternate common arm and director switches includes redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage.
Semiconductor losses	Medium	Medium	Low	Low
Applications	Point-to-point HVDC links with rated power up to 1000MW	Point-to-point and multi-terminal HVDC systems with rated power up to 1000MW and dc voltage up to 640kV.	Point-to-point and multi-terminal UHVDC systems with rated power up to 3000MW and dc voltage up to 800kV	Point-to-point and multi-terminal UHVDC systems with rated power up to 3000MW and dc voltage up to 800kV
Remarks	Offers most features of MMCs with asymmetric bipolar cells.	Offers all features of MMCs with asymmetric bipolar cells.	Offers most features of MMCs with symmetric bipolar cells.	Offers most features of MMCs with symmetric bipolar cells.

Table 7-3: High-level comparison of dc-dc converters for HVDC applications [58, 65, 97, 120-124]

	Non-isolated F2F	Isolated F2F	Partially isolated	Non-isolated MMC	Non-isolated hybrid cascaded
DC voltage matching	Yes	Yes	Yes	Yes	Yes
DC voltage and power control	Yes	Yes	Yes	Yes	Yes
Control flexibility	Normal	Normal	High	Normal	Normal
DC fault containment	Stops pole-to-pole (P2P) dc fault from spreading to healthy side, but unable to prevent pole shifting as a result of pole-to-ground (P2G) dc fault.	Stops P2P dc fault from spreading to healthy side, and prevents pole shifting in the healthy side as a result of P2G dc fault.	Stops P2P dc fault from spreading to healthy side, and prevents pole shifting in the healthy side as a result of P2G dc fault.	Stops P2P dc fault from spreading to healthy side, and prevents pole shifting in the healthy side as a result of P2G dc fault.	Stops P2P dc fault from spreading to healthy side, and prevent pole shifting in the healthy side as a result of P2G dc fault.
Power losses	Very high	High	low	moderate	Moderate
Cost	Very high	High	moderate	moderate	moderate

Table 7-4: High-level comparison of series power flow controllers [74, 76, 78-80]

	Controlled series resistor	Interline series power flow controllers	Isolated series voltage injection
Control range	Control dc line power flow in one direction	Control dc line power flow in both directions	Control dc line power flow in both directions
Power losses	low	low	Relatively high
Complexity (circuit and control)	low	Low, thanks to low-voltage rated IGBTs and capacitors	Relatively high (two back-to-back converters and isolation transformers)
Vulnerability to dc faults	Manageable	Manageable	Manageable
Cost	low	High	moderate

Table 7-5: High-level comparison of low loss dc circuit breakers [18, 78, 87, 91, 93, 99, 100, 125-140]

	Hybrid dc circuit breakers	Resonance based dc circuit breakers
Target operating speeds	3ms to 5ms	8ms to 15ms, except type 4 dc circuit breaker in Fig. 7(d)
Cost	High, because of their large semiconductor areas	Relatively low, because of their relatively low semiconductor areas.
Current breaking capacity	Relatively low (semiconductor switches of the breaking branch restrict its current breaking capability); therefore, relatively large dc inductors are needed to slow the rate of rise of dc fault currents.	High; but, large dc inductors are needed to slow the rate of rise of dc fault currents and extend the fault clearance time, without posing risk to semiconductor switches of the converters.
Footprint	Large, mostly dominated by semiconductor devices	Relative small due to small semiconductor areas

## 8. CONCLUSIONS

Recognizing its limitations, LCC-HVDC links could act as backbones for highly complex power grids, so that they can operate with nearly constant power, meaning that the required power balancing and frequency control function could be performed by VSC-HVDC links, some of the generators and other FACTS devices.

HB-MMCs and its variants are expected to dominate HVDC parts of future smart grids due to their high efficiency and fault tolerant circuit structure, which can facilitate continued operation during internal faults (cell failures) and resiliency to ac network faults. This is enabled by recent progress in the dc circuit breakers developments (summarised in Section 7). There are a number of established and successful methods available that allow the HB-MMC and its variants to survive a dc fault for extended periods prior to opening of the dc circuit such as diversion of part or the entire fault current to thyristors or mechanical switch. However, successful isolation of the faulty part, while ensuring uninterrupted power exchange through the healthy parts of the HVDC network, relies on the incorporation of large dc inductances in order to prevent rapid collapse of the dc voltage in the healthy parts; thus, slowing down the dc fault propagation within the dc network.

FB-MMCs and its inferior derivatives (from a control aspect) offer a solution for less critical power corridors in future power grids, where the entire dc network which is affected by a dc short circuit fault could be allowed to briefly stop operation. During this, dc fault clearance can be done using fast disconnectors or ac circuit breakers, and the system could afterwards be reenergised quickly from the ac grids or stored energy in the converters' cell capacitors in a controlled manner. In such a scenario, the dc fault current could be extinguished rapidly by a brief period of negative polarity dc voltage injection. Additionally, these converters can prevent exposure of the healthy pole to twice the rated dc voltage during a pole-to-ground dc fault (pole restraining); thus, facilitating continued operation during a pole-to-ground dc fault. These power converter groups could be designed for a customized level of fault tolerant operation against semiconductor losses.

DC-DC converters are essential for proper operation of highly meshed MT-HVDC networks (power flow optimization, dc voltage matching and segmentation of large MT-HVDC networks into several protection zones). F2F dc-dc converters offer all these features but at a high level of losses and cost as both its converters and transformer have to be rated for 1pu power. Non-isolated or partially isolated auto dc transformers offers dc voltage matching and power flow optimization at reduced semiconductor loss and cost. But they compromise the dc fault protection offered by the F2F topology. This means, cost effective dc auto-transformers could be used in less critical power corridors of smart grids.

Series type power flow controllers such as in Fig. 5 offer the possibility for optimizing dc power flow in highly meshed MT-HVDC networks without excessive power loss and the high cost of dc-transformers (dc-dc converters).

## 9. ACKNOWLEDGEMENT

This work is part of contribution of University of Strathclyde and SINTEF Energi to European Energy Research Alliance (EERA), sub-programme 5, Review of Transmission Technologies for Smart Grids.

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