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Control Methods for Fault Current Limiting Using Hybrid HVDC Breakers

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SUMMARY

This paper studies the integration of fault current limiting mode of hybrid HVDC breakers (HHB) with dc grid protections and HHB internal controls. Fault current limiting is particularly beneficial in case of delayed protection operation in outer zones. This might happen for a range of reasons like: slow HVDC breakers, breakers (temporary) not ready, or (temporary) protection failure.

It is proposed to use two signals to communicate between HHB and relay: 1) K_{inner} denoting request for tripping because of fault in inner zone, and K_{outer}, request for fault current limiting because of protection system delays/problems. The paper discusses the options for enabling and disabling fault current limiting mode. HHB may enter current limiting mode either by grid order or based on its own measurements. It may exit current limiting mode either in open status or in closed status depending whether external fault has been cleared or not. The study shows that HHB has inherent property of exiting in closed status on fault clearing even if there is no external signal, which improves system reliability.

A 3-line, single node, 320kV DC system is used for PSCAD simulations. Simulation results illustrate several typical cases of fault current limiting with exiting in closed and in open status. It is concluded that fault current limiting is beneficial since current magnitudes are substantially reduced for delayed protection operation in outer zones.

An analytical model for energy dissipation in surge arresters is also presented for both normal breaker opening and fault current limiting mode. This model is used to analyse current limiting mode depending on the size of energy absorbers.

KEYWORDS

HVDC transmission, DC Transmission Grids, DC Circuit Breakers, DC Grid protection.

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INTRODUCTION

DC transmission grids would potentially bring numerous benefits by combining advantages of dc power transmission with flexibility of traditional meshed AC transmission grids [1]. The protection system is still one of the key technical challenges for dc grid development, although lot of research has been completed on protection components, topology and algorithms.

HHB (Hybrid HVDC Breaker) offers very fast operation, low on-state losses and has been demonstrated as high voltage prototype [2]. Another important property of this breaker type is fault current limiting [3]. Reference [3] illustrates how HHB and its fault current limiting can be used to decouple two protection zones in a large dc grid. The fault current limiting can also be beneficially used for energising dc lines, in which case HHB performs role of a pre-insertion resistor [4].

However, most studies on dc grid protection consider HHBs as switches, while application of fault current limiting has not been much studied. It is not clear how this functionality will be used to the best advantage. There is a need to investigate integration into dc grid protection and the limitations of this functionality in order to gain more confidence in the new technology.

This paper studies the HHB control methods for limiting dc fault current, the entry and exit options into this mode, interface demands on protection relays, dependency of this method on parameters including a thorough study of the energy in surge arresters.

I. HYBRID HVDC BREAKERS

A. *Structure and operation principle of semiconductor-based hybrid HVDC breaker*

Figure 1 shows the structure of semiconductor-based hybrid HVDC Breaker [2]. The load branch conducts nominal load and the initial fault current, and is composed of an ultra-fast disconnector (UFD) and a load commutation switch (LCS). The main breaker branch includes *n* breaker cells (*n=4*, with 80kV rated cells in the prototype) in series. Each breaker cell is composed of number of semiconductor devices (e.g. IGBT) with an appropriate SA (Surge Arrester) across it. The series inductor L_{dc} limits the rise of fault current while the residual current breaker (RCB) is used to break the residual current. Detailed description of the HHB can be found in [2] and [3].

It is noted that two control signals are proposed as inputs to HHB from the relay:

- K_{inner} (denoting fault in inner zone) which immediately trips HHB,
- K_{outer} (fault outside protection zone), which initiates fault current limiting.

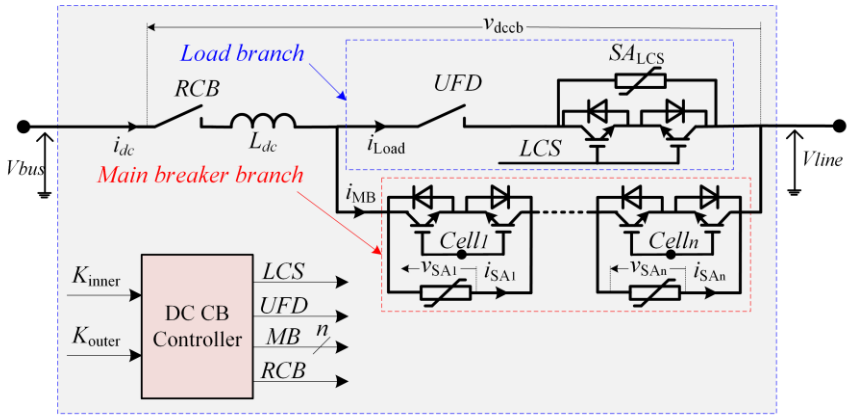


Figure 1. Structure of IGBT-based hybrid breaker

II. FAULT CURRENT LIMITING MODE

Semiconductor-based HHB has fault current limiting capability because the series breaker cells in the main branch can be controlled independently. The fault current on a particular line can be regulated at a desired level by continuously switching cells in and out. It is noted that such limiting would be required on each feeding DC line, in order to fully control current through the fault path.

A. *Local control of fault current*

Figure 2 shows block diagram of current limiting control algorithm. The measured direct current is compared with user defined current limiting reference value I_{refCL} and PI controller processes the error. The output of the PI controller is discretized and conditioned (hysteresis) to determine the number of breaker cells to be switched in. An energy balancing algorithm, similar to capacitor voltage balancing in MMC, is used to keep the surge arresters' dissipated energy balanced. Arrester energy is estimated using current and voltage measurements [5]. A higher switching frequency (f_{sw} =2kHz in the test system) enables better current regulation and better energy sharing across the surge arresters at the cost of higher junction temperature of the IGBTs. The current limiting time is constrained by the energy capacity of the surge arresters and the junction temperature of the IGBTs.

The current limiting reference I_{refCL} can be a constant value (typically around 1pu) or perhaps a gradually declining to zero with a pre-determined slope or manipulated by higher level controls.

Lower I_{refCL} reduces the energy dissipation while higher current reference has advantage of faster recovery and easier detection of faults on outer lines.

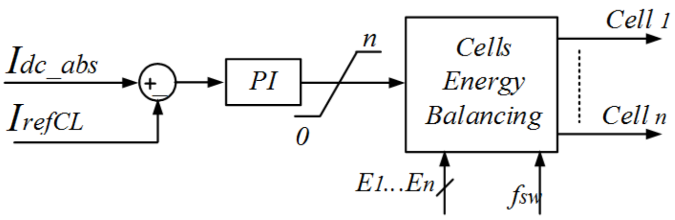


Figure 2. Controller for current reference tracking and energy balancing in cells.

B. *Entering fault current limiting mode*

The fault current limiting mode can be enabled by receiving K_{outer} signal from the grid protection relay (K_{outer} =0 enabled, K_{outer} =1 disabled). This may happen if:

- another relay (on another dc line) or central bus/substation protection device sends enabling signal. As an example when a fault is detected, the relay can send a trip signal to local HHB (K_{inner}) and send another signal (K_{outer}) to all the other HHBs on the lines connected to the same dc bus.
- local measurement is used. As an example, low dc bus voltage is a good indicator that there is a fault in an outer zone. Over current might be another signal which indicates a fault in either outer or inner zone. In case of relay failure, local overcurrent signal could activate current limiting.

C. *Exiting fault current limiting mode*

The current limiting mode can either end up with the closed status or the open status of the HHB. The final status can be open if:

- K_{inner} signal changes to zero. This will indicate presence of fault in inner zone, or it can be requested from outer relays as a backup protection.
- Self-protection on either semiconductor temperature or energy limit in surge arresters. The actual threshold values will depend on the project requirements like the length of operation in current limiting mode and the design trade offs. .

or closed if:

- K_{outer} signal changes to one. This indicates that outer fault has been cleared. The signal change may be initiated by outer relay (the other breaker on the same dc bus has already interrupted the fault) or by local measurement (bus voltage has recovered).
- Automatically. The current limiting mode maintains the current at a reference value in feedback manner. When external fault is cleared all voltages are high, cable currents will reduce, and the only way to keep current at reference is to have all switches closed (all arresters bypassed). This means that the final close status is achieved automatically.

D. *Integration of fault current limiting with HHB inner controls*

Figure 3 shows the possible flowchart of opening sequence with fault current limiting. It is seen that the breaker starts opening sequence if it receives a grid level order or based on its own local measurement. The normal opening is in fact a special case of current limiting where I_{refCL}=0.

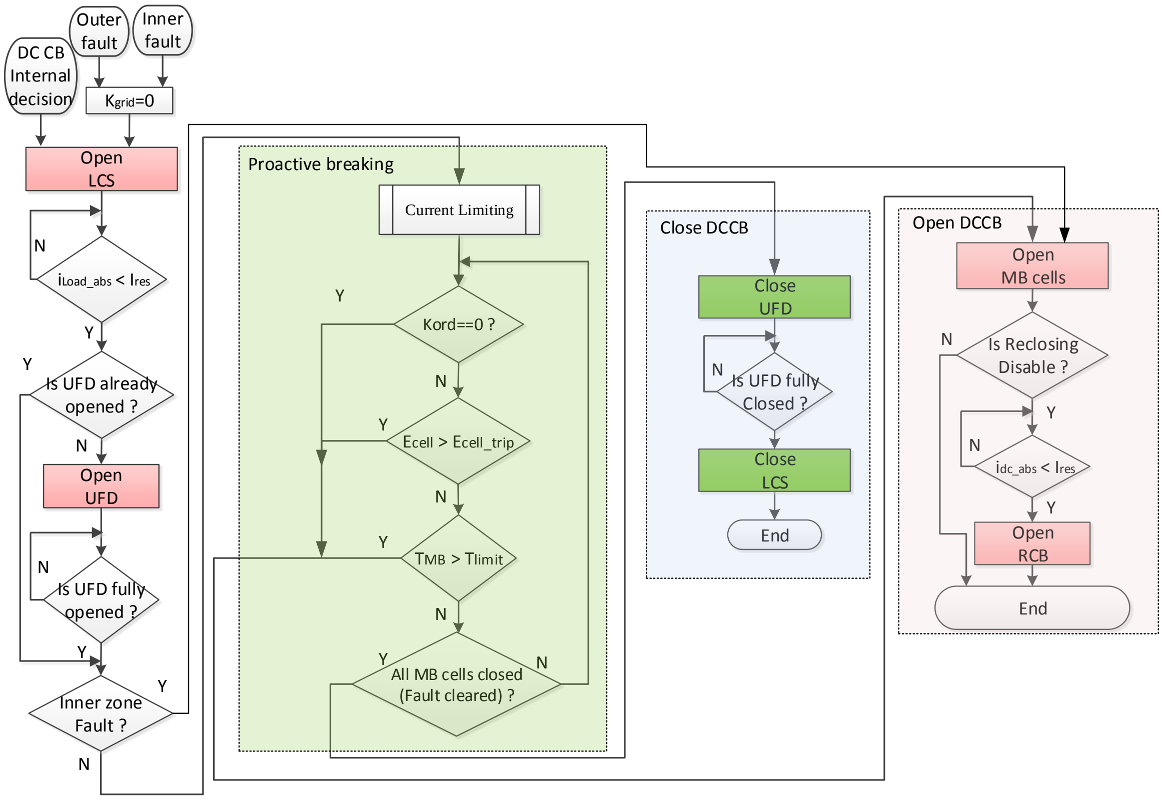


Figure 3. Opening control sequence with current limiting integrated.

E. *Surge arrester energy calculation*

Figure 4 shows a typical fault current pattern with current limiting. Fault happens at time t_0 and a trip signal is sent to the breaker at $t=t_1$. Four time regions are defined:

1. T_1: All SAs are off.
2. T_2: All SAs are switched in.
3. T_3: SAs are continuously switched in and out (current limiting mode).
4. T_4: All SAs are switched in.

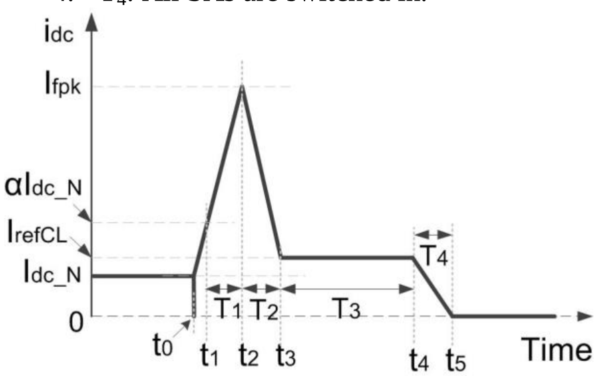


Figure 4. Fault current pattern with current limiting

The energy dissipation of each SA can be calculated by integrating its power loss over time as

$$E_{SA} = \int_0^t v_{SA} i_{SA} dt \qquad (1)$$

Since all SAs are off during period T_1, $E_{SA\_T1}=0$. With reference to Figure 1, assuming the breaker V_{bus} is connected to a stiff dc source equal to nominal dc voltage $V_{bus}=V_{dcN}$, and a low impedance fault happens at the line side $V_{line}=0$, the fault current reaches peak value I_{fpk} after T_1 which is calculated as:

$$I_{fpk} = \alpha I_{dcN} + \frac{T_1 V_{dcN}}{L_{dc}} \tag{2}$$

where T_1 is the breaker operation time [6] and αI_{dcN} is the fault current magnitude at trip decision $t=t_1$.
The energy dissipation of each SA during T_2 (E_{SA_T2}) depends on peak fault current I_{fpk} and duration T_2. Assuming that the fault current decays linearly from I_{fpk} to I_{refCL} during T_2 and the clamping voltage across each SA is constant: $V_{SA\_clamped}=1.5V_{dcN}/n$, where *n* is the number of series cells:

$$E_{SA\_T2} \approx \int_{t_2}^{t_3} V_{SA\_clamp} i_{SA} dt \approx \frac{3}{2n}\left(I_{fpk}^2 + I_{refCL}^2\right) L_{dc} \tag{3}$$

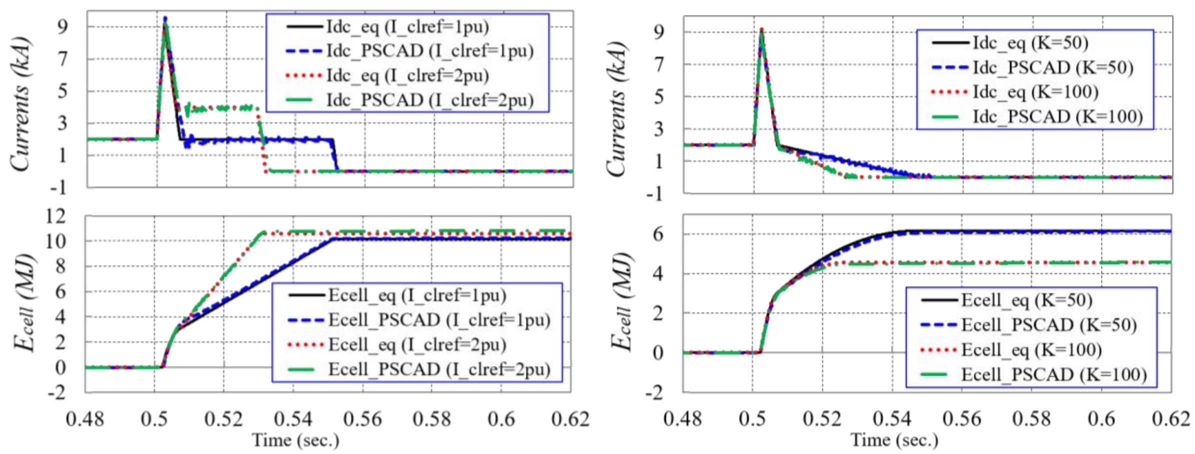
During T_3, the SAs are continuously switched in and out, and the energy is:

$$E_{SA\_T3} \approx \int_{t_3}^{t_4} \beta V_{SA\_clamp} I_{refCL} dt = \frac{V_{dcN}}{n} I_{refCL} T_3 \tag{4}$$

Where $0<\beta=T_{SA\_IN}/T_3<1$ and T_{SA_IN} is the time that SA is switched in (or equivalently the IGBT valve is switched off). T_{SA_IN} and T_3 depend on I_{refCL} and fault condition.
In case that the reference current is linearly decaying to zero during T_4, the E_{SA_T4} is calculated as

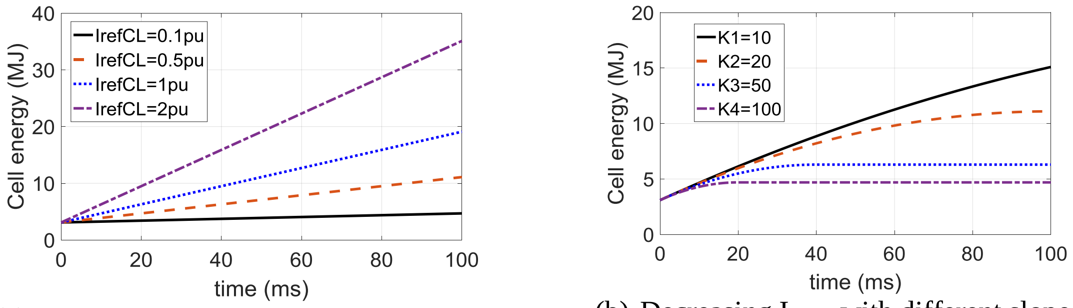
$$E_{SA\_T4} \approx \int_{t_4}^{t_5} V_{SA\_clamp} i_{SA} dt = \frac{3}{2n} I_{refCL}^2 L_{dc} \tag{5}$$

Figure 5 shows the comparisons of the above formulae with the values obtained using PSCAD simulation, which confirms model accuracy. The responses in this figure should be regarded as typical but approximate, while actual curves will depend on the particular project. In Figure 5a) various values of constant current reference are considered while in Figure 5b) K denotes slope of decaying current. The breaker parameters are given in Table I, and the breaker is connected to a dc source while fault resistance is 0 Ω.
Figure 6 shows the SA energy depending on the duration of fault current limiting mode for the same breaker as in Figure 5. These figures enable estimation of required SA energy for given fault current limiting duration period and reference current (or vice-versa). To obtain the total HHB energy, the values in Figure 6 should be multiplied by number of cells (e.g. n=4 in the test system).



a)constant current reference b) decaying current reference

Figure 5. Verification of analytical expressions for energy and current.



(a) Constant I_{refCL} (b) Decreasing I_{refCL} with different slope

Figure 6. SA energy vs time duration of current limiting mode

F. IGBT junction temperature calculation

The junction temperatures of semiconductor switches are calculated based on the thermal model from [7] and considering data for the latest BIGT semiconductors [8]. The thermal impedance Z_{thJC} (between junction and case) is composed of four parallel first order filters. LCS is assumed water cooled, while the main breaker is air cooled. The environment temperature T_0 is selected as 40ºC for LCS and 35ºC for BIGT valves in the main breaker. The BIGT power loss, P_{loss} , consists of conduction and switching loss. The switching loss P_{loss_sw} is calculated based on the energy loss for single turn ON/OFF and the switching frequency (f_{sw}) while the conduction P_{loss_cond} loss is:

$$
\begin{aligned}
P_{loss}(t) &= P_{loss\_cond}(t) + P_{loss\_sw}(t) \\
P_{loss\_cond}(t) &= V_{CE0} \cdot i_{IGBT}(t) + R_{ON} \cdot i_{IGBT}^{2}(t)
\end{aligned}
\tag{6}
$$

where R_{on} and V_{CE0} are respectively the ON resistance and forward drop voltage of each BIGT switch.

III. ADVANTAGES OF FAULT CURRENT LIMITING AND INTEGRATION INTO DC GRID PROTECTION

A. Applications of fault current limiting

Each dc line in a complex dc grid may employ different breaker technologies and/or different protection algorithms. HHB is a relatively fast topology in comparison to mechanical-based breakers and enables fault current limiting commencing in 2-4 ms. Fault current limiting can be particularly beneficial when a DC fault happens outside the protection zone of the protecting device i.e. hybrid HVDC breaker. Current limiting has the following potential applications and advantages:

- In case of slow breakers on other lines, the current limiting mode can be enabled before the slow breakers operate. This means that current infeed and energy in slow breakers will be reduced. Slower breakers may be installed on the other dc lines (in the outer protection zones) because of financial advantages. The best effect is achieved if all feeding lines have HHB.
- In case of delays in protection operation on other lines. Some breakers may require lockout time to regain "ready" state after certain events. This time delay may be caused by the need to recharge capacitors for injecting current, or recharge driving circuits for high-force generators (Thomson coils), or need to reduce temperature in some breaker components.
- Permanent or temporary protection failure on other lines. Current limiting provides more time for protection system by reducing the current infeed to the faulty line. This gives opportunity for repeated protection attempts/restarts on other lines.
- Repeated open-close on other lines. New protection algorithms may require repeated open-close in a short time. It increases current and voltage stresses on breakers. Fault current limiting will reduce stresses and will limit inrush currents on other lines.

Figure 7 shows a possible method for protection decisions in relays, assuming fully local decision making. Two output signals are present, which is consistent with breaker model in Figure 1:

1. K_{inner} (denoting fault in inner zone) which is activated with selective protection algorithm. Rate of change of line voltage (ROCOV) is shown in the figure, as used for simulation.

2. K_{outer} (fault outside protection zone), which is activated by undervolted on the bus-side (V_{bus}).
It is noted that Kouter will be activated only in case of delays in external protection. In normal operation the outer fault will be cleared sufficiently fast and Kouter will not be activated.

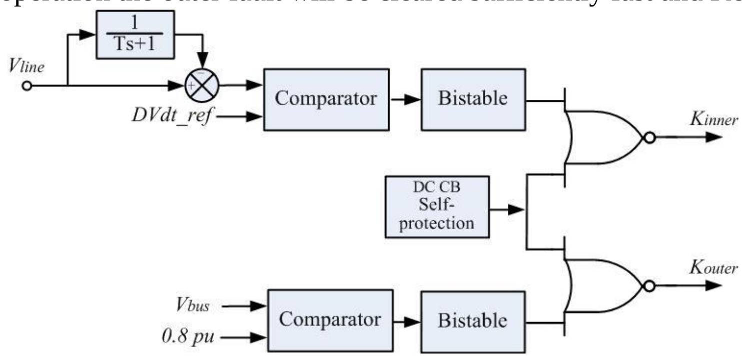


Figure 7. Basic protection algorithm with fault current limiting

IV. SIMULATION RESULTS

A. *Simulation system*

Figure 8 shows the schematic of the simulation model which represents a bus of a dc grid where the rest of the grid is represented by stiff dc voltage sources. All three breakers are HHB type. Table I summarizes the system main parameters. Distributed parameter DC cable models are used. The HHB model, including fault current limiting is reported in [5]..
A number of simulation cases including different conditions to enter and exit breaker current limiting have been investigated. However, only key results are reported here for brevity.

B. *No fault current limiting*

Figure 9 shows the simulation of a fault on line 2, where total time between fault initiation and opening of main breaker in HHB 2 (protection time plus breaker operating time) is extended to 5.5ms. There is no fault current limiting at any of breakers. It is seen that the peak current on line 2 is high (15kA), and HHB2 temperature and energy are also reaching high values. The current in the healthy lines 1 and 3 also reach high values. If protection delay is any longer then current may exceed HHB2 rating, and there is danger that HHB1 and HHB3 might trip on self-protection, depending on settings [5].

C. *Exit in open state based on E_{SA}*

Figure 10 shows the results with current limiting exiting to open status based on energy dissipation of SA (higher than 10MJ). A fault 2 is applied at 0.5s, and HHB 2 fails to open. HHB1 and HHB3 detect low bus voltage and enter fault current limiting mode with I_{refCL}=1kA. HHB1 and HHB3 controllers are configured to exit in open state when energy in any SAs exceeds 10MJ, which according to the analytical model enables around 120ms of fault current limiting.
It is seen in Figure 10a) that currents in lines 1 and 3 are regulated to 1kA, while current in line 2 is their sum (2kA). The peak current in line 2 is 5.5kA, and then it is maintained at 2kA for 120ms.
Figure 10 b) shows that line voltages of cables 1 and 3 are maintained high, at the rated value of 320kV for the duration of current limiting. This is one of practical advantages of this operating mode.

Table I simulation circuit parameters and HHB main parameters (same for all 3 lines)

Parameter	V_{dcN}	I_{dcN}	I_{fpk}	L_{dc}	T_1	n	f_{sw}
Value	320 kV	2 kA	16 kA	100 mH	2 ms	4	2kHz

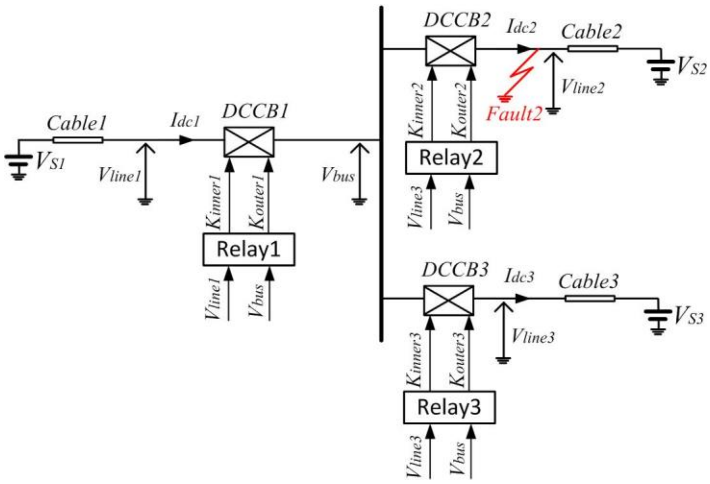


Figure 8. Schematic diagram for simulated test system.

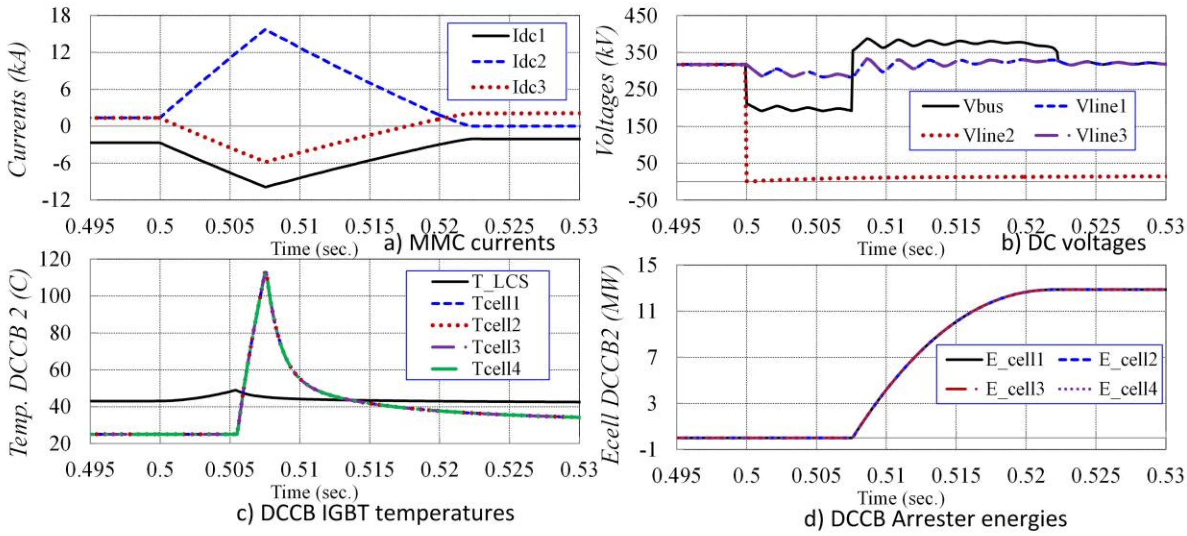


Figure 9. Fault on line 2 with HHB 2 total opening time of *10ms*. There is no fault current limiting on any line.

Figure 10c) shows the temperatures in LCS and T2 valves in each of the three HHBs. LCS temperatures do not increase since the load path conducts for a very short time. It is seen that the temperature of the main valves raises to around 60deg, which is well below the rated value of 120deg, for the 120ms long current limiting period. This shows that valve temperature is not the constraining factor in this design.

Figure 10d) shows the energies in each SA in the three HHBs. As energy increases to 10MJ, HHB is commanded to open. It is also seen that energies are well balanced between the 4 SAs in each HHB, confirming that energy balancing logic operates well.

D. Exit in closed state

Figure 11 shows the results with current limiting exiting to closed state, with the same fault scenario. In this case the protection delay is increased to 20 ms to better show the benefits of current limiting (delay shorter than 7.5 ms will not initiate current limiting in HHB1). Note that HHB2 current will not increase if delay is prolonged further, since all feeding lines use fault current limiting. Longer delays require only larger energy absorbers in the HHBs.

It is seen that HHB1 and HHB3 enter current limiting mode after 2.5 ms and 7.5 ms, respectively. At 0.522 ms the bus voltage recovers indicating that fault is cleared. Immediately afterwards HHB1 and HHB3 exit in closed status and currents return to nominal values. It is seen that energy dissipation and temperature rise are modest in this short current limiting interval.

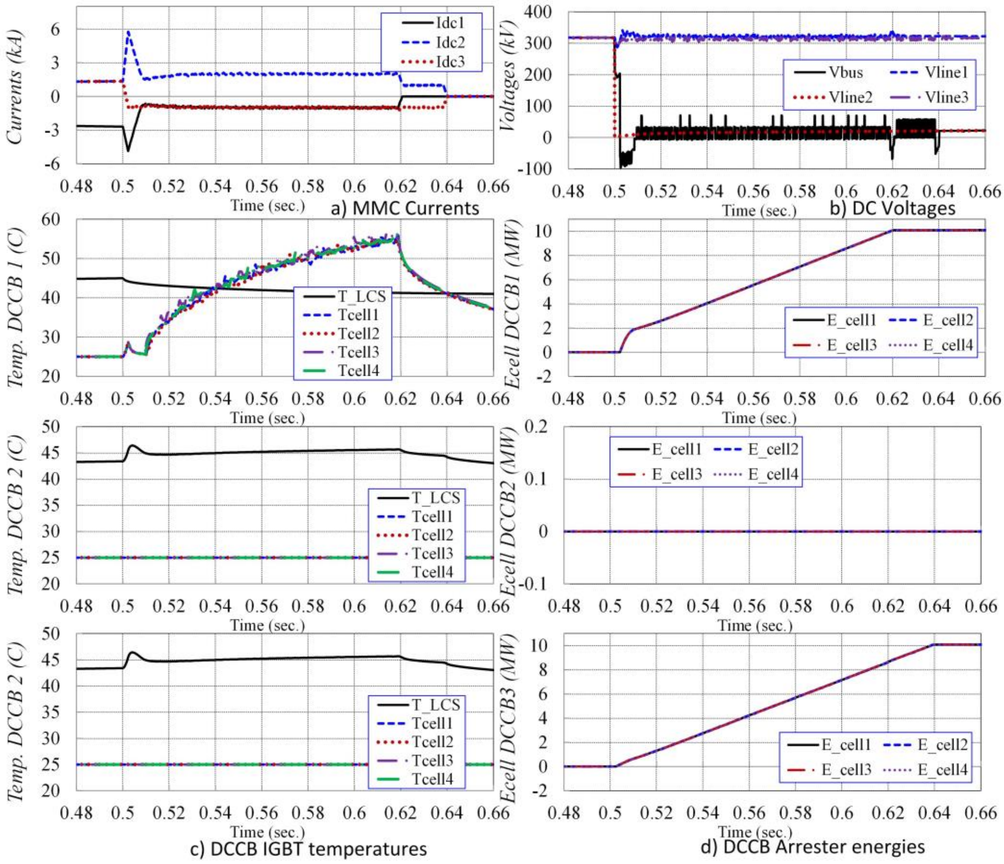


Figure 10. Fault on line 2 where HHB 2 failed to open, and with fault current limiting on lines 1 and 3. Exit is in open state because of 10MJ energy limit in each surge arrester.

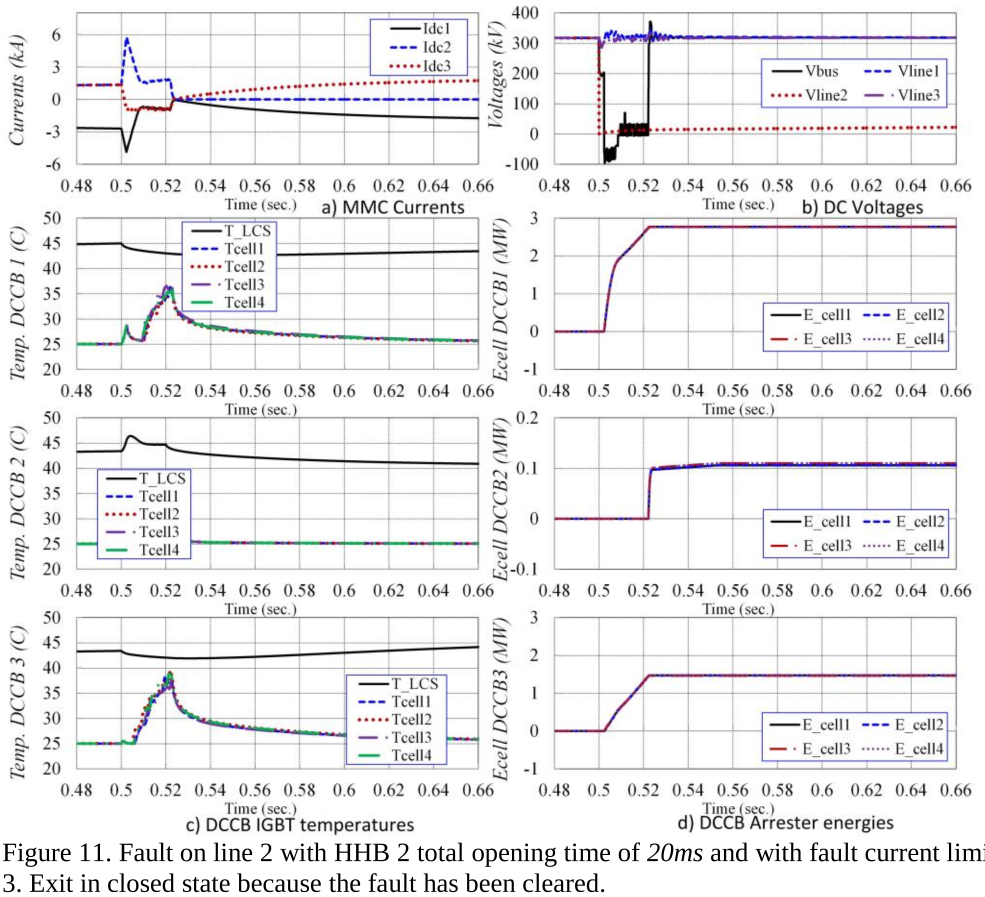


Figure 11. Fault on line 2 with HHB 2 total opening time of *20ms* and with fault current limiting on lines 1 and 3. Exit in closed state because the fault has been cleared.

It is emphasized that the above benefits (limiting fault current) are evident because of the test system employed. The test system has HHBs with current limiting installed on all lines. If for example one dc line has no current limiting device then such line would feed high fault current and there is smaller benefit of limiting current on other lines.

V. CONCLUSIONS

The fault current limiting operating mode with hybrid HVDC breaker can be particularly useful for protection failure or delayed operation on external dc lines. It is concluded that HHB requires two controls inputs from the relay: one for tripping and another one for initiating current limiting. Entering current limiting mode can be initiated either by external relays or by local measurements. Exit from current limiting is possible in open state or in closed state depending if the external fault has been cleared or not.

The simulation results have illustrated benefits of fault current limiting on a 3-line single node simulation model, for cases with slow protection on other dc lines. It is concluded that current limiting reduces current infeed into a fault, and provides additional time for slow protection system.

The analytical model for energy dissipation enables estimation of duration of current limiting operation depending on current reference.

VI. ACKNOWLEDGEMENTS

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VII. BIBLIOGRAPHY

[1] D Jovcic and K Ahmed "High-Voltage Direct Current Transmission: Converters Systems and DC Grids", Wiley 2015.

[2] Häfner, J., Jacobson, B.: 'Proactive Hybrid HVDC Breakers - A key innovation for reliable HVDC grids'. Proc. CIGRE 2011 Bologna Symp. Bologna, Italy, Sep 2012, pp. 1-7.

[3] Frans Dijkhuizen, Bertil Berggren "Zoning in High Voltage DC (HVDC) Grids using Hybrid DC breaker" EPRI HVDC and FACTS Conference, Palo Alto, August 2013.

[4] Vinothkumar K, Inger Segerqvist, Niclas Johannesson, Arman Hassanpoor "Sequential Auto-Reclosing Method for Hybrid HVDC Breaker in VSC HVDC Links " IEEE SPEC power electronics conference, Auckland, December 2016

[5] W Lin, D.Jovcic, S.Nguefeu and H Saad "Modelling of High Power Hybrid DC Circuit Breaker for Grid Level Studies", IET Power Electronics, Vol. 9, issue 2, February 2016, pp 237-246.

[6] CIGRE joined WG A3 and B4.34 "Technical Requirements and Specifications of State of the art HVDC Switching Equipment" CIGRE brochure 683, April 2017

[7] S. Rohner, S. Bernet, M. Hiller, and R. Sommer, "Modulation, Losses, and Semiconductor Requirements of Modular Multilevel Converters", IEEE Trans. Ind. Electronics, 2010, 57 (8), pp. 2633-2642.

[8] Liutauras Storasta at all "Optimized Power Semiconductors for the Power Electronics Based HVDC Breaker Application" PCIM Europe, Nuremberg, May 2015.