Selecting frequency and parameters of DC-fault tolerant Non-Isolated high power MMC DC/DC Converter

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ABSTRACT:
This paper studies MMC-based non-isolated DC/DC converter for DC transmission grids. The key design parameters including operating frequency and size of passive components are evaluated with the aim of ensuring DC fault tolerance and minimizing losses and size. An analytical model is used to perform parametric studies while detailed non-linear model is used for verification. The case study on 600MW, 320kV/250kV system reveals the narrow range of optimal cell capacitance and arm inductance while lower-side arms require substantially larger capacitors. With the targeted losses of 1.5%, and voltage ripple of ±5%, it is recommended to use around 150Hz operating frequency. For the offshore applications, higher frequency enables significantly smaller size with some increase in losses. The line inductor on the low-voltage side should be much larger than the arm inductor and plays a key role in the dc fault responses.

1. Introduction

DC/DC converters are expected to play significant role in future DC transmission grids [1]-[4]. CIGRE has studied DC/DC converters in building DC grids [5], as power flow controllers [6], and recently WG B4.76 dedicated to DC/DC has been stablished. In general, they interconnect two DC systems with different (or equal) voltage levels and can also provide additional attractive features like bidirectional power flow control, DC fault isolation, stabilization and multi-vendor interconnection [1]. There are two main families of DC/DC converters; (i) isolated which are based on two-stage DC/AC/DC conversion, and (ii) non-isolated converters (NIDCCs), which use a newer technology with single-stage DC/DC conversion.

There is only a limited information on the non-isolated DC/DC converters (NIDCCs) design and control [7]-[10], which are all based on MMC (Modular Multilevel Converter) topology, and these initial studies have been focused on demonstrating the concept and developing simple models. The study in [7] considers a low-power 14MW 17kV/3kV DC/DC with 2.5kHz operating frequency, while [8] demonstrates 3kW, 50Hz hardware design. The study in [9] compares multiple designs from 15MW to 1.21GW however only basic analysis is provided and the topology includes unnecessary passive components. Reference [10] develops phasor model for a 7MW 8.8kV/4.4kV at 350Hz operating frequency. The recent publication from CIGRE WG B4.76 [11] proposes a 600MW 320/250kV NIDCC test case and concludes that the components and ratings will be comparable to a similar MMC AC/DC converter.

These recent publications raise expectations that a non-isolated MMC DC/DC potentially offers very cost-effective method of interchanging power between two HVDC systems and could be more attractive than using the isolated DC/DC converter in some scenarios. However, none of the references analyses design principles, component stresses/selection, performance and DC faults for GW-size NIDCCs at HVDC transmission voltages.

This article aims to provide an in-depth analysis of design trade-offs of a practical NIDCC rated 500MW-1000MW with voltages around 320kV. The principal design aims are:

- Bidirectional controllable power flow,
- DC fault blocking capability on both DC sides,
- Minimizing costs, size, weight and power losses

Assuming topology as adopted by CIGRE B4.76 [11], the parameters that can be manipulated to achieve these goals include: Number and topology of MMC cells, phase number, operating frequency, cell capacitance, arm inductance, line inductance and modulation techniques. In general, most parameters affect multiple design goals.

The analytical model will be employed for essential parameter studies. It is necessary to consider DC power flow, but also fundamental and harmonic AC variables which facilitate power balancing between phase arms. The conclusions will be verified on a detailed PSCAD model.

The contribution of this article is the analytical and systematic design methodology illustrated on a realistic test case. Although iterative design process will be adopted, the method is still significantly faster and more revealing comparing with traditional parameters tuning using EMT simulation. An important further conclusion is the confirmation of DC fault tolerance.

2. Non-Isolated MMC DC/DC Converter

2.1. Converter structure

Fig. 1 shows the structure of a three-phase NIDCC enabling power transfer between HV DC grid V1 and LV DC grid V2 [1], [11]. Each phase is composed of two arms. In order to determine the peak voltage stress on arms, it is necessary to consider normal operation and also DC faults on each side. Fig. 2 shows the equivalent circuits for (worst-case) faults on each of the two DC terminals (V1 and V2, where V1>V2), and it indicates the voltage stress on each arm.

Table 1 summarizes the peak arm voltage stress, where V_{armAC} is the AC component [1]. Each lower arm includes NL half-bridge submodules (HBSM). The upper arms have NU cells, but a number of these should be full-bridge submodules (FBSM) to provide at least -V2 voltage for V1 faults.

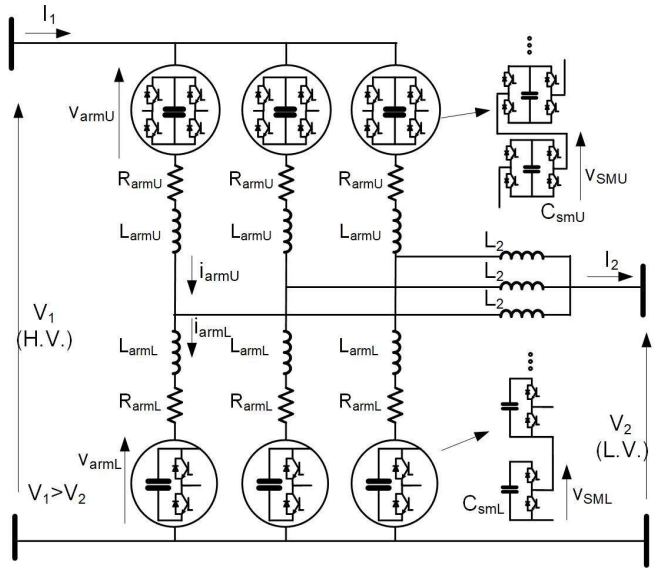

Fig. 1. *Three-phase NIDCC*

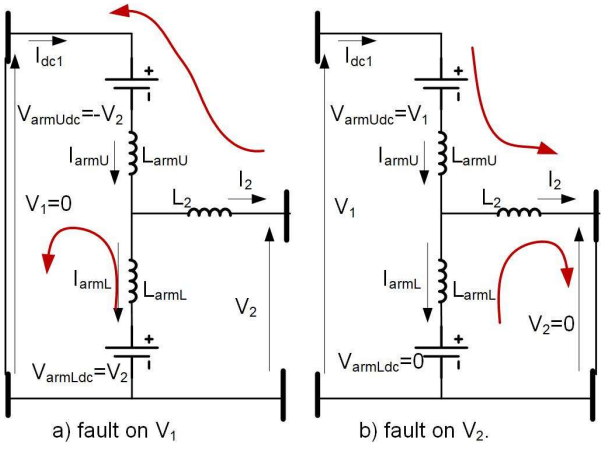

Fig. 2. *Equivalent circuit for DC faults*

Table 1 Arm voltage stresses

	Normal operation	V1 fault	V2 fault
Upper arm	V_1-V_2+V_{armU_AC}	-V_2	V_1
Lower arm	V_2+V_{armL_AC}	V_2	0

2.2. Converter analytical steady-state model

The dynamic equations of the NIDCC are studied in [1], [7] and only a summary is given. The equations for current, sum arm voltages, and arm voltages are:

$$\frac{di_{armU}}{dt}=\frac{-L_{yL}}{L_Z}v_{armU}-\frac{L_2}{L_Z}v_{armL}-\frac{L_{yL}R_{armU}}{L_Z}i_{armU}-\frac{L_2R_{armL}}{L_Z}i_{armL} \quad (1)$$

$$\frac{di_{armL}}{dt}=-\frac{L_2}{L_Z}v_{armU}-\frac{L_{yU}}{L_Z}v_{armL}-\frac{L_2R_{armU}}{L_Z}i_{armU}-\frac{L_{yU}R_{armL}}{L_Z}i_{armL} \quad (2)$$

$$\frac{dv^{\Sigma}_{armU}}{dt}=\frac{1}{C_{armU}}m_{armU}i_{armU} \quad (3)$$

$$\frac{dv^{\Sigma}_{armL}}{dt}=\frac{1}{C_{armL}}m_{armL}i_{armL} \quad (4)$$

$$v_{armU}=m_{armU}v^{\Sigma}_{armU} \quad (5)$$

$$v_{armL}=m_{armL}v^{\Sigma}_{armL} \quad (6)$$

Where the parameters are defined as:

$$\begin{aligned} &L_z=L_2\left(L_{armU}+L_{armL}\right)+L_{armU}L_{armL},\\ &L_{yU}=L_2+L_{armU}, L_{yL}=L_2+L_{armL},\\ &C_{armU}=\frac{C_{SMU}}{N},\quad C_{armL}=\frac{C_{SML}}{N} \end{aligned} \quad (7)$$

All the variables are assumed to include DC component, fundamental component and second harmonic. The arm voltages can be expressed as:

$$\begin{aligned} v_{armU}&=V_{armU\_dc}+V_{armU\_ac}\cos\left(\omega t\right)+V_{armU2\_ac}\cos\left(\omega t+\theta_{vU2}\right)\\ v_{armL}&=V_{armL\_dc}+V_{armL\_ac}\cos\left(\omega t+\theta_{vL}\right)+V_{armU2\_ac}\cos\left(\omega t+\theta_{vL2}\right) \end{aligned} \quad (8)$$

where the average arm voltages (neglecting losses) are:

$$V_{armU\_dc}=V_1-V_2,\quad V_{armL\_dc}=V_2, \quad (9)$$

Similarly, the upper and lower arms sum voltage are:

$$\begin{aligned} v^{\Sigma}_{armU}&=V^{\Sigma}_{armU\_dc}+V^{\Sigma}_{armU\_ac}\cos\left(\omega t+\theta^{\Sigma}_{vU}\right)+V^{\Sigma}_{armU2\_ac}\cos\left(\omega t+\theta^{\Sigma}_{vU2}\right)\\ v^{\Sigma}_{armL}&=V^{\Sigma}_{armL\_dc}+V^{\Sigma}_{armL\_ac}\cos\left(\omega t+\theta^{\Sigma}_{vL}\right)+V^{\Sigma}_{armL2\_ac}\cos\left(\omega t+\theta^{\Sigma}_{vL2}\right) \end{aligned} \quad (10)$$

The average value of sum voltage should equal at least the expected arm voltage stress which according to Table 1 is

$$V^{\Sigma}_{armU\_dc}=V^{\Sigma}_{armL\_dc}=V_1 \quad (11)$$

Correspondingly, the upper, lower and L2 currents are:

$$\begin{aligned} i_{armU}&=I_{armU\_dc}+I_{armU\_ac}\cos\left(\omega t+\theta_{iU}\right)+I_{armU2\_ac}\cos\left(\omega t+\theta_{iU2}\right)\\ i_{armL}&=I_{armL\_dc}+I_{armL\_ac}\cos\left(\omega t+\theta_{iL}\right)+I_{armL\_ac2}\cos\left(\omega t+\theta_{iL2}\right)\\ i_{L2}&=I_{L2\_dc}+I_{L2\_ac}\cos\left(\omega t+\theta_{L2}\right)+I_{L22\_ac}\cos\left(\omega t+\theta_{iL22}\right) \end{aligned} \quad (12)$$

where the average currents are by inspection:

$$I_{armU\_dc} = \frac{I_1}{3}, \quad I_{armL\_dc} = \frac{I_1 - I_2}{3}, \quad I_{L2\_dc} = \frac{I_2}{3} \tag{13}$$

The control signals are assumed to have DC and fundamental components as:

$$\begin{aligned} m_{armU} &= M_{U\_dc} + M_{U\_ac}\cos(\omega t) \\ m_{armL} &= M_{L\_dc} + M_{L\_ac}\cos(\omega t + \theta_{vL}) \end{aligned} \tag{14}$$

These components will be determined in the controller. However neglecting losses, from (5), (6), (9) and (11) the DC components of the control signals are derived as:

$$M_{U\_dc} = 1 - \frac{V_2}{V_1}, \quad M_{L\_dc} = \frac{V_2}{V_1}, \tag{15}$$

The AC voltages are maximized to reduce current [11]. Considering that $m_{armU}<1$ and $m_{armL}<1$, from (14) and (15) the maximum AC modulation indices are:

$$M_{U\_ac} = M_{L\_ac} = \min\left(M_{U\_dc}, M_{L\_dc}\right) \tag{16}$$

As analyzed in [1] and [7] the power transfer between upper and lower arms is equal to:

$$P_{ac} = \frac{M_{L\_ac}\sin\theta_{vL} M_{U\_ac}\left(V^{\Sigma}_{armU\_dc}\right)^2 L_2}{\omega L_z} \tag{17}$$

The DC model is given in (5), (6), (9), (11), (13) and (15). The above model at fundamental and second harmonic frequencies is converted to DQ frames, as it is described for AC-DC MMC converters in [1] and [12]. The dynamic components are replaced with reactances to obtain a phasor-type model [12]. The model gives DC, DQ fundamental and DQ second harmonics for each of the 7 variables: upper and lower sum arm voltages, arm voltages and arm currents, and L2 currents. It enables parametric studies which are considerably faster than time-domain simulation on PSCAD models.

3. Test case design of NIDCC

The design is carried out for a test case 600MW NIDCC with V_1=320kV and V_2=250kV, which is expected to be typical DC/DC in future DC grids [11]. The design aim is to minimise components while limiting the losses to around 1.5% and cell voltage ripple to ±5%.

3.1. Number of phases

For a given power, the number of phases and the rating of semiconductors in valves are related. Generally, higher number of phases reduces the valves current and provides higher reliability but increases the system cost and size. Fig. 3 shows the upper and lower arms peak current versus NIDCC rated power for three different numbers of phases. It is seen that for the rated power of 600MW, a three-phase NIDCC would be suitable if 2kA IGBT module is selected (for ex. IGBT module ABB 5SNA 2000K450300 [13]).

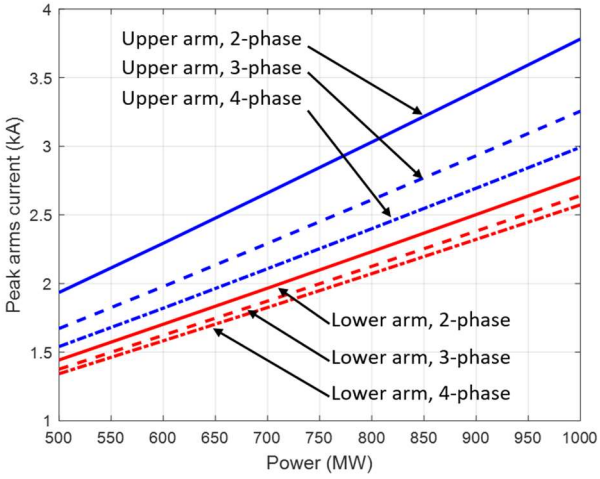

Fig. 3. *The upper and lower arms peak current versus rated power for 3 different numbers of phases*

3.2. Submodule capacitance

Larger capacitor size gives lower SM voltage ripple but increases the overall cost, size and weight. The voltage ripple on the sum arm voltage is considered as the sum of fundamental and second harmonics:

$$\begin{aligned} \Delta V_{SM\_U} &= \sqrt{\left(V^{\Sigma}_{armU\_ac}\right)^2 + \left(V^{\Sigma}_{armU2\_ac}\right)^2} \\ \Delta V_{SM\_L} &= \sqrt{\left(V^{\Sigma}_{armL\_ac}\right)^2 + \left(V^{\Sigma}_{armL2\_ac}\right)^2} \end{aligned} \tag{18}$$

Fig. 4 and Fig. 5 show the capacitors voltage ripple versus the upper and lower arms SM capacitance (assuming L_2=80mH) and three different arm inductances. It is seen that:

- The upper (lower) arms voltage ripple decreases by increasing the upper (lower) arm capacitance.
- In some parameter range, one capacitance change affects ripple on both (upper and lower) arms.
- Arm inductance also affects voltage ripple but in a complex and non-linear manner.
- Lower arms require higher capacitance. The fundamental component (which is dominant) of voltage ripple is much larger on the lower arms despite the fact that lower and upper arms have similar fundamental component currents. This is explained considering DC component of modulation which directly affects voltage ripple [1]. Since $M_{L\_dc}>M_{U\_dc}$ the lower arm voltage has higher ripple at fundamental harmonic.
- To enable ±5% voltage ripple on both arms, the following components are recommended: C_{smU}=1,760 µF, C_{smL}=12,000 µF, $L_{armU}=L_{armL}=L_{arm}$=11 mH.

The above study is repeated for a range of frequencies, and capacitance values for ±5% ripple are noted. Fig. 7 shows the upper and lower arms SM capacitance versus the operating frequency.

As expected, higher frequency lowers capacitance size. However, the curves are very steep for frequencies below 300Hz which implies possible significant size/cost savings by optimizing design in this frequency range. There seems to be

minimal benefit of increasing frequency over 800Hz or increasing arm inductors over 20mH.

3.3. Arm inductance

The arm inductors in MMC are required to maintain current while cells are inserted, to limit the AC (fundamental and harmonic) currents and to limit rise of the dc fault current.

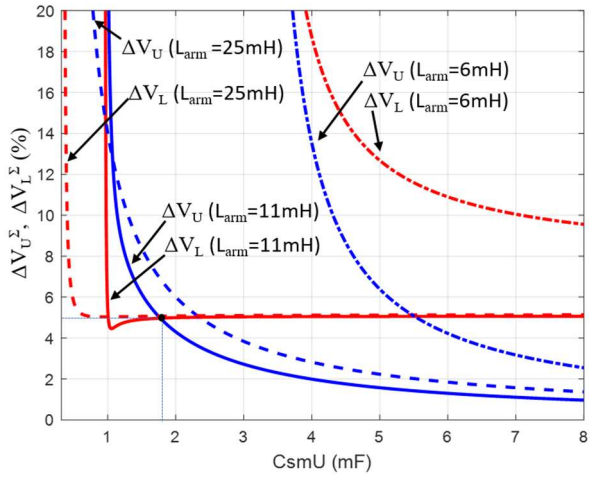

Fig. 4. *The upper (ΔV_U^{Σ}) and lower (ΔV_L^{Σ}) arm sum voltage ripples versus upper arms SM capacitance, (f=150Hz, C_{smL}=12,800μF, L_2=80mH)*

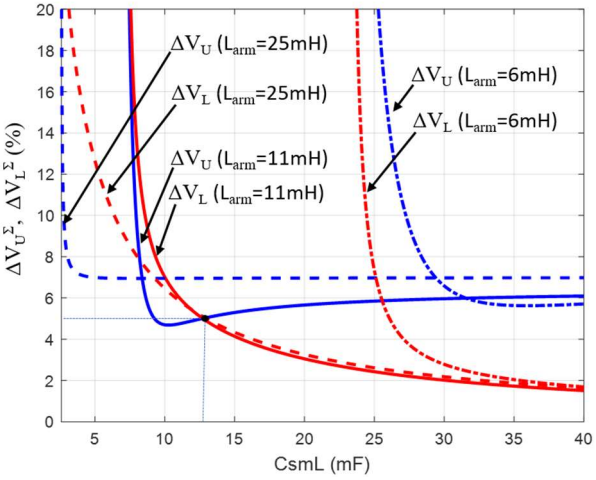

Fig. 5. *The upper (ΔV_U^{Σ}) and lower (ΔV_L^{Σ}) arm sum voltage ripples versus lower arms SM capacitance, (f=150Hz, C_{smU}=1,760μF, L_2=80mH)*

Fig. 6 shows the impact of arm inductance on the upper, lower and L_2 RMS currents, and also on the cell capacitance. The line inductance L2 is kept equal to 80mH, frequency is initially f=150Hz and cell voltage ripple is maintained at ±5%. The arms RMS currents are calculated as:

$$I_{armU} = \sqrt{\left(I_{armU\_dc}\right)^2 + \left(I_{armU\_ac}\right)^2}$$
$$I_{armL} = \sqrt{\left(I_{armL\_dc}\right)^2 + \left(I_{armL\_ac}\right)^2} \qquad (19)$$
$$I_{L2} = \sqrt{\left(I_{L2\_dc}\right)^2 + \left(I_{L2\_ac}\right)^2}$$

It is seen that the AC currents are different on upper/lower arms despite the fact that AC modulation indices, sum arm voltages and parameters are identical. This is the result cross of coupling between variables in DC, fundamental and second harmonics. The AC currents on upper and lower arms would be obtained as identical if simple fundamental frequency model from [1] and [7] was used. Fig. 6c) shows the angle between AC voltages of upper and lower arms assuming full power transfer (600MW). As arm inductances increase the power transfer decreases (required angle becomes larger) because of lower currents and higher reactance as it is seen in (17). The theoretical maximum angle is 90 deg, but it is necessary to maintain sufficient control margin and therefore maximal values of 30-50deg are adopted.

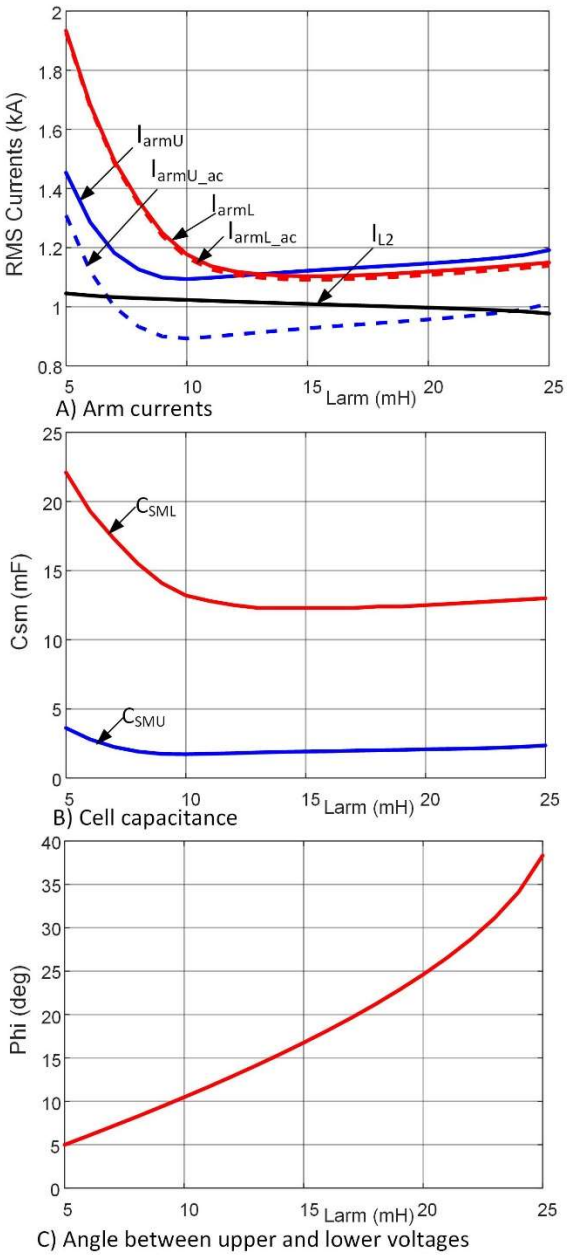

Fig. 6. *Impact of arm inductance, (f=150Hz, L_2=80mH, $\Delta V_U^{\Sigma}=\Delta V_L^{\Sigma}$ =±5%)*

It is seen that both the arms RMS current and cell capacitance decrease steeply for L_{arm}<10mH. The value of

arm inductance also determines the second harmonic current, which is illustrated in Fig. 8. In conventional AC-DC 50Hz MMC converters a dedicated second harmonic suppression control is employed since second harmonics may reach high values. Fig. 8 illustrates that second harmonic in the test NIDCC is low (below 3%), because of the higher operating frequency, and second harmonic controller may not be needed.

3.4. L_2 inductance

The inductor L_2 is required to moderate the arms/L_2 currents and also to limit the dc fault current (which is analyzed in section 5Fig. 9 shows the upper, lower arms and L_2 RMS currents versus L_2 inductance. In general, larger L_2 is better, however the obtained L_2 values are quite significant, and therefore L_2 size/weight and also losses should be considered.

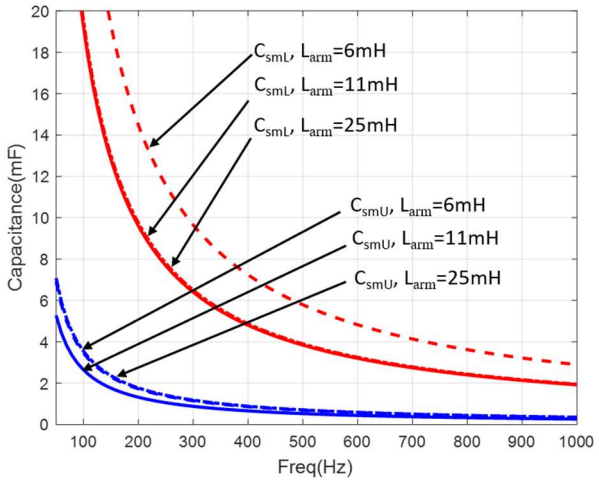

Fig. 7. *The required upper/lower arms SM capacitance versus operating frequency, ($\Delta V_U^{\Sigma}= \Delta V_L^{\Sigma} =\pm 5\%$, L_2=80mH)*

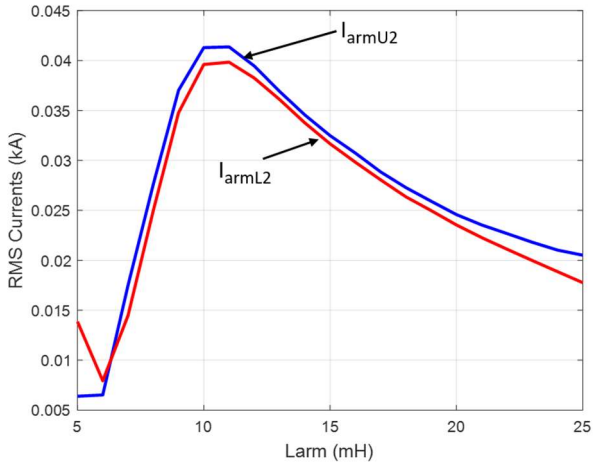

Fig. 8. *The arms second harmonic currents versus arm inductance, (f=150Hz, C_{smU}=1760μF, C_{smL}=12,800μF, L_2=80mH, $\Delta V_U^{\Sigma}= \Delta V_L^{\Sigma} =\pm 5\%$)*

3.5. Power Losses

Three NIDCC loss components are considered: arms and L_2 inductors losses, valve conduction losses, and valve switching losses.

The inductors conduction loss can be calculated by considering the resistance and the RMS currents:

$$P_{loss\_L} = 3R_{Larm}\left(I_{armU}^2 + I_{armL}^2\right) + 3R_{L2}\left(I_{L2}^2\right) \quad (20)$$

where I_{armU}, I_{armL} and I_{L2} are RMS value of currents, and R_{arm} and R_{L2} are the respective inductors resistance. The inductors resistance depends on the material, length and cross section diameter and is taken as 5 mΩ/mH [15].

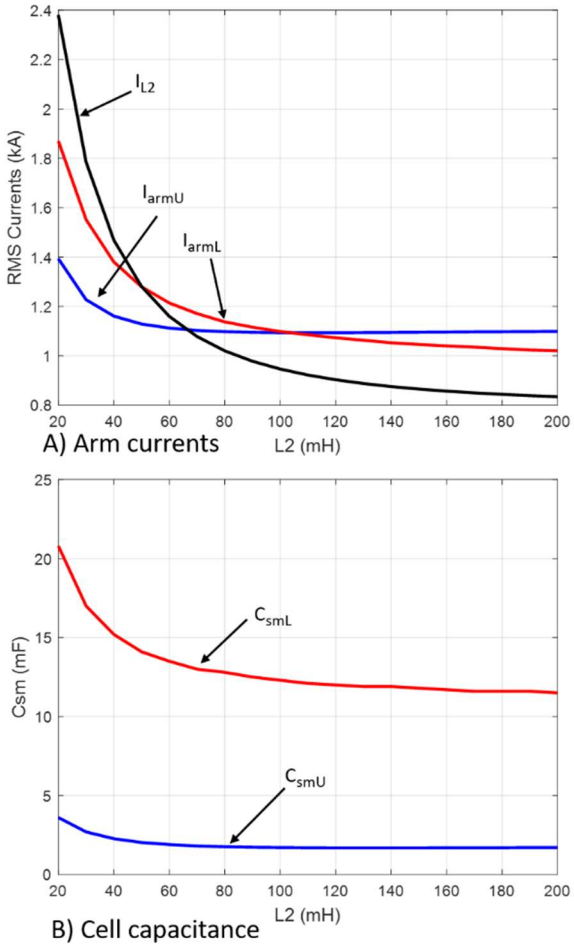

Fig. 9. *The impact of L_2 inductance, (f=150Hz, L_{arm}=11mH, $\Delta V_U^{\Sigma}=\Delta V_L^{\Sigma}=\pm 5\%$)*

The conduction loss of a HBSMs can be calculated using

$$P_{Cond\_HBSM} = \left(\rho_{S1} + \rho_{S2}\right)P_{Cond\_S} + \left(\rho_{D1} + \rho_{D2}\right)P_{Cond\_D} \quad (21)$$

where $\rho_{S1,2}$ and $\rho_{D1,2}$ are respectively the ratios that the switches S1, S2 and diodes D1 and D2 of a HBSM conduct the arm current in one cycle. These ratios depend on power transfer direction and voltage balancing algorithm and on average they are assumed equal i.e. $\rho_{S1}=\rho_{S2}=\rho_{D1}=\rho_{D2}=25\%$. The P_{Cond_S} and P_{Cond_D} are respectively the conduction loss of a switch and diode and are given by

$$P_{Cond\_S/D} = u_{ON\_S/D} I_{arm\_ave} + r_{ON\_S/D} I_{arm}^2 \quad (22)$$

where I_{arm_ave} and I_{arm} are respectively the average and RMS values of the upper/lower arms current, and $u_{ON\_S/D}$ and $r_{ON\_S/D}$ are respectively the threshold voltage and ON

resistance of switch/diode, which can be obtained from the IGBT datasheet.

The total switching energy for a switching cycle for one switch is equal to the sum of the turn-on, turn-off switching energies Eon and E_{off} and the reverse recovery energy E_{rec}. Assuming r switching in a cycle, the switching loss is:

$$P_{SW\_HBSM} = r \times f \times \left(E_{on}\left(I_{arm}\right) + E_{off}\left(I_{arm}\right) + E_{rec}\left(I_{arm}\right)\right) \quad (23)$$

In this study, two switching per cycle are assumed r=2 considering nearest level control [1]. The conduction/switching loss of a FBSM is selected as 50% higher than the conduction/switching loss of a HBSM [13].

The losses are calculated for wide range of parameters while maintaining ±5% voltage ripple. Fig. 10 shows the power loss versus Larm and L_2 inductances. It is seen that there is significant impact on loses in the parameter range L_{arm}<8mH and L_2<80mH, and importantly the curves show parabolic shape.

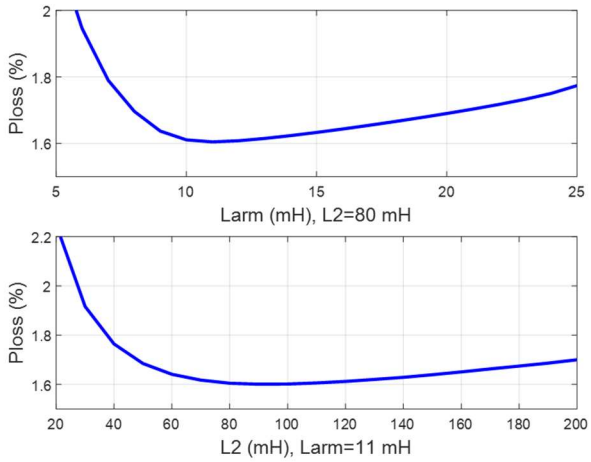

Fig. 10. *The power loss versus arm and L2 inductances, (f=150Hz, $\Delta V_U^{\Sigma} = \Delta V_L^{\Sigma} = \pm 5\%$)*

4. Operating frequency

The research studies worldwide have indicated that the operating frequency for GW-size DC/DC should be selected in the range of 100Hz-500Hz [13]. Higher operating frequency decreases the size of SM capacitors and the arms (and L_2) inductors. On the downside, it increases the switching loss, and also increases the computational burden and could make voltage balancing challenging if the number of SMs is high.

Table 2 summarizes the impact of different operating frequencies on the NIDCC parameters and losses while the SMs voltage ripple is kept at around ±5%. There are many design options, and for simplicity arm currents are also maintained identical (corresponds to same IGBT switches) at around 1.1 kA RMS.

By increasing the operating frequency, the size of L_{arm}/L_2 inductors and SM capacitors decrease linearly and directly in proportion with frequency, but the power loss increases at a lower rate. If the converter size is a major concern (like in offshore applications), a higher operating frequency in the range of 300Hz-500Hz should be selected. However, for other applications and considering the size, cost and power loss, the operating frequency of 150Hz-200Hz is recommended. It is important to conclude that say 150Hz NIDCC converter would be expected to have only 30-50% higher losses and costs compared to a similar (600MW) AC-DC MMC converter.

Table 2. NIDCC parameters and losses for different operating frequencies

Freq. (Hz)	C_{smU} (μF)	C_{smL} (μF)	C_{smU}+C_{smL} (kJ/MVA)	L_{arm} (mH)	L_2 (mH)	P_{loss} (%)
50	5280	38400	69.9	33	240	0.98
100	2640	19200	34.9	16.5	120	1.24
150	**1760**	**12800**	**23.3**	**11**	**80**	**1.55**
200	1320	9600	17.5	8.25	60	1.88
300	880	6400	11.7	5.5	40	2.54
400	660	4800	8.74	4.12	30	3.21
500	528	3840	6.99	3.3	24	3.88
600	440	3200	5.83	2.75	20	4.55
800	330	2400	4.37	2.06	15	5.90
1000	264	1920	3.50	1.65	12	7.25

5. DC fault considerations

It is desired that a dc fault at each side of the converter is isolated and the fault current should not propagate to the other side. This can be achieved by properly dimensioning valves as illustrated in Fig. 2. However, considering that the fault detection and blocking of IGBTs may take time, the arm (and L2) inductors should be sufficiently large to limit the initial rise of the dc fault current. As a common rule, the maximum one-off IGBTs turn-off current is 2pu.

The following assumptions are made for the dc fault study:

- The NIDCC controller does not react in the considered time frame and therefore modulation indices are maintained constant.
- The sum arm voltage is maintained constant. These two assumptions imply that the average upper and lower arms dc voltages are constant (V_1-V_2 and V_2).
- The remote source voltages V_1 and V_2 are constant, assuming worst-case strong DC grids.
- The fault has low impedance; i.e. R_f=0
- The fault detection and blocking IGBTs time T_d is much shorter than one period T=1/f to neglect the arms ac voltage changes during T_d.

If a low impedance fault happens on HV side at time t=t_0, the upper and lower arm fault currents are approximated by:

$$I_{fHV\_armU} = \frac{T_d\left(v_{armL}(t_0)\dfrac{L_2}{L_{armL}+L_2} + V_2\dfrac{L_{armL}}{L_{armL}+L_2} + v_{armU}(t_0)\right)}{\left(L_{armU} + L_{armL} \parallel L_2\right)} - i_{armU}(t_0)$$

$$I_{fHV\_armL} = \frac{T_d V_1}{\left(L_{armU} + L_{armL}\right)} - i_{armL}(t_0) \quad (24)$$

Similarly, for a low impedance dc fault on the LV side:

$$I_{fLV\_armU} = \frac{T_d\left(V_1 - v_{armU}(t_0)\right)}{\left(L_{armU} + L_2\right)} + i_{armU}(t_0)$$
$$I_{fLV\_armL} = \frac{T_d v_{armL}(t_0)}{\left(L_{armL} + L_2\right)} - i_{armL}(t_0) \quad (25)$$

It is seen that the arms fault currents depend on the converter parameters, and also the arms currents and voltages at t_0 (the fault instant). These initial values can be obtained by running time-domain simulation, or a simplified method can be used, as presented below.

From (5), (6), (8) and (14), and by ignoring the fundamental and second harmonic terms of the sum arms voltages (i.e., $v^{\Sigma}_{armU} \approx v^{\Sigma}_{armL} \approx V_1$), the time-domain arms voltages can be approximated by

$$v_{armU}(t) \approx (V_1 - V_2) + (V_1 - V_2)\cos(\omega t)$$
$$v_{armL}(t) \approx V_2 + (V_1 - V_2)\cos(\omega t + \theta_{vL}) \quad (26)$$

where the lower arm voltage phase angle θ_{vL} can be determined from (17).

By ignoring the arms resistances and the second harmonics components of the arms currents, the fundamental ac components of the arms currents in steady-state phasor domain are obtained from (1) and (2) as

$$\begin{bmatrix} i_{armU\_ac} \\ i_{armL\_ac} \end{bmatrix} = \begin{bmatrix} j\frac{L_{yL}}{\omega L_Z} v_{armU\_ac} + j\frac{L_2}{\omega L_Z} v_{armL\_ac} \\ j\frac{L_2}{\omega L_Z} v_{armU\_ac} + j\frac{L_{yU}}{\omega L_Z} v_{armL\_ac} \end{bmatrix} \quad (27)$$

where v_{armU_ac} and v_{armL_ac} are the second terms of (26). The approximated arms currents are then obtained from (12) by ignoring the second harmonic terms and replacing the fundamental frequency terms from (27).

The approximated arms voltages and currents are replaced in (24) and (25) and the fault time t_0 (within one period $\omega t \in [0, 2\pi]$) that gives the maximum arms fault currents is obtained. The minimum arms and L_2 inductances are then analysed to keep the maximum arms fault currents below the permissible one-off IGBTs turn-off current (2pu).

Fig. 11 shows parametric study of L_2 versus L_{arm} for two values for fault detection delay: T_d=100µs and T_d=300µs. Any pair L_2, L_{arm} values above and right of both curves (the shaded area) is acceptable to keep the fault current below 2pu. It is seen that detection time T_d<300µs is required in order to adopt the inductance range considered in the previous sections.

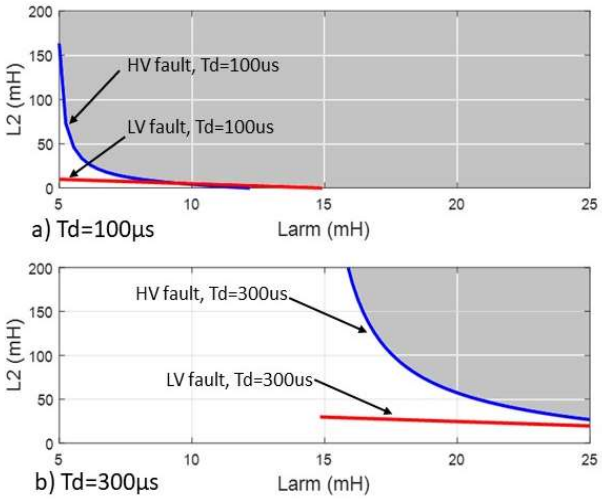

Fig. 11. *The L_2 versus L_{arm} for dc fault considerations for two different T_d*

6. Selection of final parameters

The overall procedure to determine the size of the NIDCC parameters is shown in Fig. 12. For a given rated power and voltages, the number of phases and suitable IGBT modules are first determined based on Fig. 3. The minimal value for inductors are determined based on a given fault detection time T_d (and the converter operating frequency) as illustrated in Fig. 11.

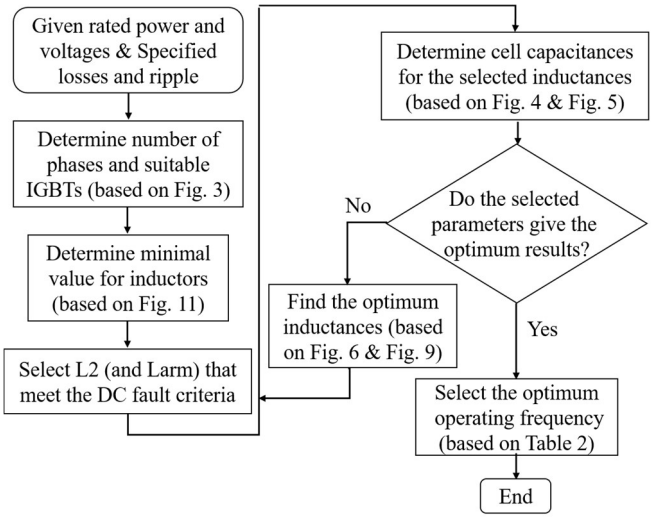

Fig. 12. *Flowchart of optimum components selection*

The inductance L_2 should be as large as practically feasible, although the practical values are expected to be an order of magnitude larger than the arm inductors and hence size/cost will be an important limitation. For the selected L_2 and L_{arm} (within the shaded area of Fig. 11), the upper and lower arms cell capacitances are obtained to keep the cell voltages ripple around ±5% (as shown in Fig. 4 and Fig. 5). It will be then checked (based on Fig. 6 and Fig. 9) if the selected inductances (and capacitances) give the optimum results. If not, the optimum value of L_2 and L_{arm} will be adjusted to minimize the size of capacitors and losses. The operating frequency is finally revised based on size, cost and power loss criteria (and also considering technical challenges).

6.1. The base test case

The selected optimum parameters with overall power loss of around 1.5% are shown in bold in Table 2. The power loss of the NIDCC with the selected parameters is calculated for lower power flows and tabulated in Table 3. It is seen that the power loss decreases by reducing the power flow. However, the reduction is not linear caused by the system nonlinearities.

Table 3. 150Hz NIDCC power loss for different power flows

Power flow (pu)	0.1	0.5	0.7	1.0
Power loss (%)	0.40	0.81	1.09	1.55

6.2. Generalization to other test cases

The design has been carried out for NIDCC with a different range of frequencies, powers and voltages and the results for cases are summarized in Table 4. The last column shows the pu impedance for the arm and L_2 inductances which are obtained by dividing their impedance (at the operating frequency) by the base impedance Z_{base}. The base impedance is obtained as $Z_{base}=V_{ac}^2/P$ where the V_{ac} is rms value of the arms ac voltage ($(V_1-V_2)/\sqrt{2}$) for both arms. It seen that the pu impedance for the arm and L_2 inductors are almost the same for different frequencies and powers. However, scaling parameters for different DC voltage levels using pu approach may not give optimum results.

Table 4. NIDCC parameters different frequencies, powers and voltages

P (MW)	Freq. (Hz)	V_1/V_2 (kV)	C_{smU}/C_{smL} (mF)	L_{arm}/L_2 (mH)	Z_{Larm}/Z_{L2} (pu)
600	150	320/250	1.76/12.8	11/80	2.55/18.5
600	50	320/250	5.28/38.4	33/240	2.55/18.5
600	300	320/250	0.88/6.4	5.5/40	2.55/18.5
400	150	320/250	1.22/8.2	16/120	2.47/18.5
800	150	320/250	2.29/18.1	8/60	2.46/18.5
600	150	400/250	3.7/4.1	30/230	2.38/18.2
600	150	320/160	4.5/4.65	34/260	2.36/18.0

7. NIDCC design verification

A non-linear PSCAD 150Hz NIDCC model with the parameters in Table 2 is developed and feedback controller is used as presented in [11]. All the results and conclusions from the analytical studies are verified against PSCAD but only two representative cases will be shown.

1.1. Steady state operation

Fig. 13 shows the 5 key variables in steady-state NIDCC operation at full power. It is seen that the ripple is in agreement with Fig. 4, while magnitude of all currents are in agreement with Fig. 7 and Fig. 6.

Fig. 14 shows the same 5 variables for the case of 300Hz design. It is seen that variables are in general agreement with results in Fig. 7 and Table 2. This confirms operation with much smaller passive elements.

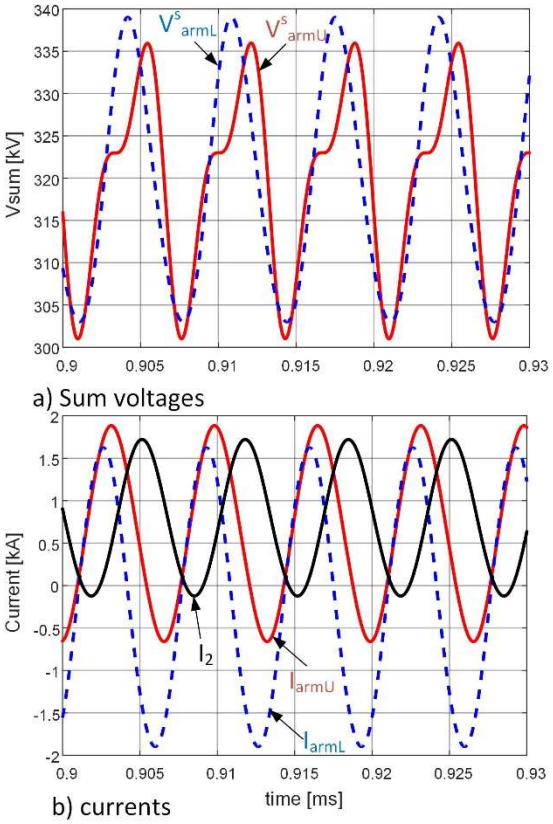

Fig. 13. *PSCAD steady-state results (f=150Hz, C_{smU}=1,760μF, C_{smL}=12,800μF, L_{arm}=11mH, L_2=80mH).*

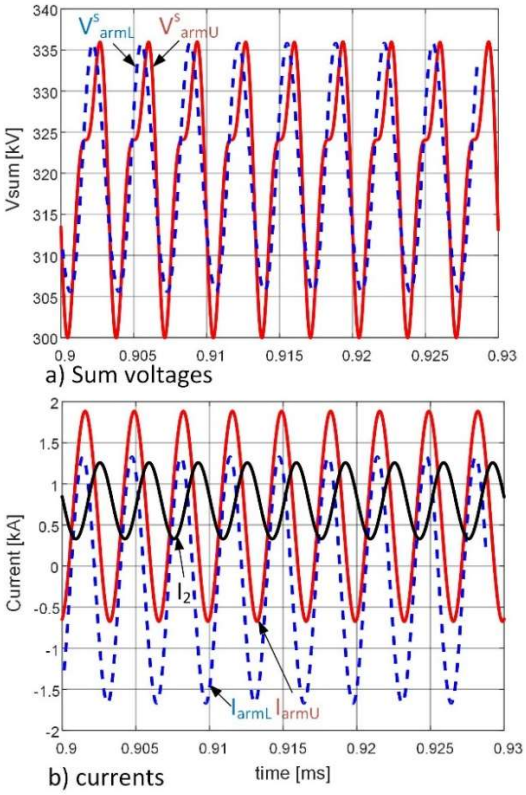

Fig. 14. *PSCAD steady-state results (f=300Hz, C_{smU}=880μF, C_{smL}=6,400μF, L_{arm}=5.5mH, L_2=40mH).*

1.2. DC fault on HV side

The MMC converter self-protection is developed on PSCAD model using two criteria: DC voltage drop below 0.8pu and arm current over 2pu. A detection delay of T_d=300µs is introduced. Fig. 15 shows that peak current is below 2pu and that the sum voltages do not deviate significantly from their nominal values as expected.

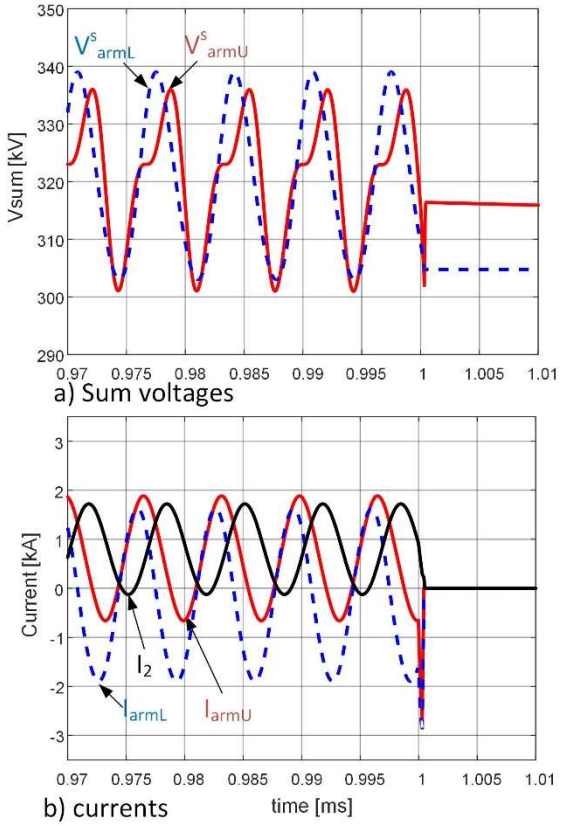

Fig. 15. *PSCAD simulation of HV-side DC terminal fault (f=150Hz).*

8. Conclusion

The study presents the optimal range for key design parameters for a non-isolated transmission-level DC/DC, rated 600MW, 320kV/250kV. There is a narrow range of optimal cell capacitance and arm inductance while arms with larger DC modulation index (lower arms in this design) require substantially larger capacitors. Larger inductors reduce size of capacitors and losses. However too large inductors may increase losses and may result in unacceptable control angle for a given power. The study shows that capacitor size on lower/upper arms affects voltage ripple on both arms in a highly non-linear way and only a limited range of values significantly reduces ripple. The optimum parameters are obtained using an iterative method while the DC fault criterion provides initial inductors size.

With the design aim of 1.5% losses and 5% voltage ripple, the optimal operating frequency would be 150Hz. For offshore applications smaller size might be required, resulting in higher frequency and higher loses. The line inductor on low-voltage side should be much larger than the arm inductor and plays a key role in dc fault responses.

The generalisation of this method using pu approach will give very good results for different power and frequency.

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