Development and Experimental Evaluation of 2 -10 kV LC DC Circuit Breaker Module

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Abstract—**The article analyses design options for a practical 2-10 kV, 1-2 kA LC DC Circuit Breaker module. The impact of multiple series break points with the ultra-fast disconnector is explored in depth using analytical model and 5 kV, 4-break hardware prototype. The experimental testing demonstrates that the arc voltage increases proportionally with each breaking point, and this increases current that can be internally commutated. Further analysis of the impact of delays between break points is presented. Modeling and testing with 4 different capacitors of 1-10 kV concludes that larger capacitances increase commutating current, but relationship is complex and non-linear. Parallel connection of breaking points is also analysed. Successful breaking of DC fault current is demonstrated on hardware for multiple cases including *930 A* with *800 µF, 6.5 kV*, capacitor using a 4-break disconnector. The tested DC CB is of mechanical type, which inserts a capacitor in series in a very short time of around *290 µs*, and full contact separation is achieved *1.5 ms* after the trip signal. It is recommended that the module design should primarily consider maximizing the number of break points in series.**

***Index Terms*-- DC switchgear, HVDC protection, DC Circuit Breakers.**

I. Introduction

DC CB (Circuit Breakers), are seen as key components in DC grids, at transmission and distribution levels [1][2]. They have been in rapid development in the past 10 years, and a good overview is provided in [3].

Hybrid DC CBs represent state of the art technology [4],[5]. They operate fast, within *2-3 ms*, but they include a high-voltage semiconductor valve which significantly increases breaker cost. They have been commercialized to high voltages and implemented in the Chinese Zhangbei DC grid and in the multiterminal Zhoushan HVDC.

Mechanical DC CBs use electromechanical components and perhaps some low-rated semiconductor valves [6], but generally have slower opening speed, of around *3-8 ms*. They too have been implemented in the Zhangbei DC grid and in the previous multiterminal NanAo HVDC.

The cost of DC CBs is significantly higher than comparable AC CBs, and is one of the impediments for further DC grid development. Also, it is much desired to improve the opening speed of the DC CBs, to reduce the peak DC fault current and passive inductors, but also to improve DC grid reliability.

The internal DC current commutation is the key challenge with DC CB design, and many options exist [7]. In all the commercialized DC CB technologies it occurs at the end of the stroke of the mechanical switch. With hybrid DC CBs, a semiconductor-based LCS (Load Commutation Switch) is employed which increases losses and costs but also lowers reliability. With mechanical DC breakers commutation occurs after prolonged (*8-10ms*) arcing while contacts are moving. Multiple recent research projects have investigated commutation at the beginning of the switch stroke [8],[9], and feasibility has been demonstrated at *1.3 kV* in [10], and *5 kV* in [11]. Such earlier commutation benefits in lowering both: peak current and energy dissipation, but in earlier studies [10], [11] the DC CB cost is high because of the use of semiconductors.

The topology called LC DC Circuit breaker, which employs only electro-mechanical components, has been demonstrated on hardware at *130A, 1.3kV* in [12]. The commutation at the beginning of disconnector stroke is achieved using solely arc voltage in around *300-500 µs*. This inserts a capacitor in series with the fault current path which then provides increasing counter voltage while the mechanical contacts are moving apart. Another advantage of LC DC CB is that arcing period is very short, of the order of tens *µs*, thus reducing thermal phenomena and contact wearing. The commutation in LC DC CB has been analysed in some depth with realistic parasitic parameters in [13], and it is shown that short disconnector arc voltage is sufficient to commutate current into a parallel capacitor. The study in [13] demonstrates *400A, 1.3kV* LC DC CB device, and it concludes that scaling of this technology to higher currents requires:

- reducing parasitic inductance in the circuit, or
- increasing capacitance, or
- increasing arc voltage,

UFD (Ultra Fast Disconnectors) are of special interest as switches because of the fastest opening speed (*2 ms* range), and have been commercialized for high voltage [14]. Switches with arcing capability have much heavier contacts resulting in lower speeds. Although UFDs have no arcing capability, the studies in [12] and [13] suggest that they are suitable for LC DC CB breakers, because of extremely short arcing time.

This article reports on the studies to advance LC DC CB concept to current levels of around *1-2 kA* and voltage levels of *2-10 kV*. We analyse the methods to increase arc voltage and in particular the benefit of using fast disconnectors with multiple

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break points. In order to understand impact of parasitics in the commutation circuit, we evaluate design of a practical module comparing several *1-10 kV* commercially available capacitors. Our analytical studies of the arc voltage and parasitics in the commutation circuit will be supported with experimental results in the University laboratory.

Section II presents the LC DC CB test system design. Section III analyses the use of disconnector with multiple breaking points. Section IV evaluates suitability of different capacitors. Section V compares the experimental results.

II. Test system LC DC Circuit Breaker design

A. LC DC CB description summary

Fig. 1 shows the topology of LC DC CB [12], and only a summary is provided here. The main components include:

- S is UFD (ultrafast disconnector), similar as in [4] and [13]. It is desired to have fast opening and negligible arcing. This switch should have contacts with lateral overlap to enable high speed at separation [12]. It may have multiple break points.
- SA is energy absorber (bank of arresters) similar as in [4]. It is rated for somewhat higher nominal DC voltage.
- C_s is parallel capacitor which is rated similarly as SA.
- S_{res} is residual switch.
- L_{dc} is required to limit the slope of current.

When the trip signal is received, *S* is commanded to open. Contacts begin to slide and conduct current until separation instant at T_o. At the separation instant contact have velocity v_o, and this enables current commutation in the capacitor C_s. The capacitor voltage will rise proportionally to the current but is limited by the capacitance. It should be lower than the gap dielectric strength, which is proportional to the gap distance. The main advantages of the circuit are:

1) The capacitor C_s replaces the main semiconductor valve in a hybrid breaker, and this brings cost benefits.
2) The voltage rise across disconnector S is limited by capacitor C_s. The commutation to the capacitor is achieved at the beginning of the disconnector contact stroke, leading to earlier insertion of counter voltage and faster fault current interruption. With hybrid DC CB [4], commutation occurs at the end of the stroke.

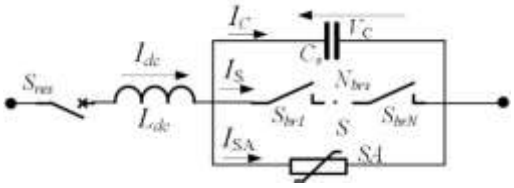

Fig. 1 LC DC Circuit Breaker with multiple break points.

B. Design objectives

This study aims to evaluate feasibility of *2-10 kV, 1-2 kA* LC DC CB unit, considering multibreak approach. Multiple break points are not widely used with arcing switches, since a single break provides the longest arc and the best opportunity for arc extinction. In our case, the arc voltage is of importance, however it is not clear how the total arc voltage depends on the number and practical implementation of breaking points.

C. UFD opening speed condition

The first design criterion is linked with the UFD opening speed. The UFD as described in [15],[13] is utilised. This device is improved by adding damping coils to reduce bounce at the end of travel. It has two moving rods, each with a contact assembly, and is driven by 4 Thomson coils. The test system parameters and all labels are given in Table I.

Under the assumption of ideal voltage sharing between N_{brs} series break points, and current sharing between N_{brp} parallel break points, the design equations from [12] can be expanded for multi-break UFD. For the given commutating current of I_0, contact velocity at separation v_0, and dielectric strength for air d_{air}, the minimal theoretical capacitance C_s value for successful commutation can be determined as:

$$v_0 d_{air} N_{brs} > I_0/(N_{brp} C_s) \tag{1}$$

This gives capacitance of $C_s>(133\mu F)/(N_{brs}N_{brp})$, which ensures current commutation assuming no parasitics in the circuit.

TABLE I Parameters of the test LC DC CB.

Label	Description .	value
T_{UFD}	UFD opening time	1.5 ms
T_o	Time to contact separation	290 µs
z_{max}	Maximum gap distance (1 break point)	3 mm
OL	Contact overlap in closed state	2 mm
d_{air}	Dielectric constant of air	3 kV/mm
v_0	Contact gap velocity at separation	5 m/s
I_0	Fault current at contact separation	2 kA
V_{dc}	Rated test circuit DC voltage	5 kV
L_{dc}	Series inductor	4.2 mH
L_1, L_2	Splitting inductors	0.2 mH
N_{brs}	Number of series break points	1,2 or 4
N_{brsp}	Number of series break points	1 or 2
V_{gap0}	Gap voltage at T_o (electrode fall)	11 V
L_{pb}	Bus bar circuit parasitic inductance	50 nH
R_{pb}	Bus bar circuit parasitic resistance	5 mΩ
L_{pc}	Capacitor parasitic inductance	varies
R_{pc}	Capacitor parasitic resistance	varies

D. Impact of parasitics on current commutation

Building on the study in [13], the analytical model for the commutation circuit with multiple break points (4 break points are shown) can be developed as shown in Fig. 2. The presence of capacitor (L_{pc}, R_{pc}) and bus (L_{pb}, R_{pb}) parasitics requires non-zero commutating voltage (arc voltage) to commutate current from switch S to capacitor C_s. Assuming equal initial gap voltage V_{gap0} (electrode fall) and simultaneous opening of all break points, the analytical expression for the peak commutated current I_{cp} and the corresponding parameters are:

$$I_{cp} = \frac{N_{brs} V_{gap0}}{Z_p} \frac{1}{\sqrt{(1-\zeta^2)}} e^{-\zeta \omega_p T_p/4} \tag{2}$$

$$Z_p = \sqrt{\frac{L_p}{C_s}}, \quad \zeta = \frac{R_p}{2Z_p} \quad \omega_p = \frac{1}{\sqrt{L_p C_s}}, T_p = \frac{2\pi}{\omega_p} \tag{3}$$

Using (2), the required arc voltage V_{gap} to break fault current I_o (equivalent to I_{cp}) can be calculated as shown in Fig. 3. Multiple values for total parasitic inductance $L_p=L_{pc}+L_{pb}$, and resistance $R_p=R_{pc}+R_{pb}$ are considered. For the considered capacitance

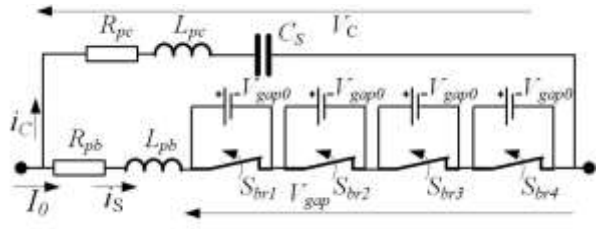

Fig. 2 Analytical model of the commutation circuit with 4 break points.

C_s=*400 μF*, assuming arc voltage on each break point *10V*<V_{gap0}<*15 V*, it is seen that we would need 10-15 break points to commutate I_o=*2 kA*. Also, it is seen that magnitude of commutating current is directly proportional to the arc voltage.

Fig. 4 shows the calculated capacitance for the required commutating current, assuming single break point V_{gap0}=*11 V*. It shows that generally higher capacitance increases the commutating current, but relationship is non-linear. All curves have parabolic shape, and the nose of the curves is pushed toward lower currents with larger resistances but toward larger capacitance with increasing inductance.

E. Impact of delays in breaking points

In practice it will not be possible to build multibreak disconnector with all breaks opening simultaneously. The peak current will be a vector sum of the current pulses from each break point. Assuming that each break point has the same arc voltage, and denoting with α_k, the delay angle [*-180,180*] of break point *k*, when scaled on the period of parasitic cycle T_p in (3), the peak commutated current from (2) can be calculated as:

$$I_{cp} = \frac{V_{gap0}}{Z_p}\frac{e^{-\zeta\omega_p T_p/4}}{\sqrt{(1-\zeta^2)}}\sqrt{\left(\sum_{k=0}^{N_{brs}} cos\alpha_k\right)^2 + \left(\sum_{k=0}^{N_{brs}} sin\alpha_k\right)^2} \quad (4)$$

This equation shows that the best outcome (largest I_{cp}) is when α_k=*0*, $\forall k$, giving arithmetic sum of all pulses, while as α_k is increasing the peak current will be lower. A sum of two unitary vectors gives magnitude larger than *1* only if the angle between vectors is in the range [*-120, 120*], and this would be maximum limit for an acceptable delay.

F. Post-commutation DC CB voltage rise

After successful commutation at T_o, the gap voltage will rise as simulated in Fig. 5 using the model from [12]. Several different capacitance values are considered, assuming I_o=*2 kA*, the circuit parameters from Table I, and considering 1,2 and 4 break points. There are two important concerns:

1. Too small capacitance will result in dielectric breakdown. The minimal capacitance is *320 μF*, *140 μF* and *70 μF*, respectively for 1, 2 and 4 break points.
2. Too large capacitance will slow voltage rise and result in lower operating speed of DC CB.

The exact expression for the time interval for capacitor voltage to reach the system voltage V_c=V_{dc} can be obtained as:

$$tan(\omega_{dc}(T_{UFD} - T_0)) < \frac{V_{dc}}{I_0}\sqrt{\frac{C_s}{L_{dc}}} \quad , \quad \omega_{dc} = \frac{1}{\sqrt{L_{dc}C_s}}, \quad (5)$$

With a single break this gives capacitance C_s<*599 μF* (I_o= *2 kA*), although this condition also depends on the inductance L_{dc}.

III. Experimental Test System

A. DC CB testing system

The test circuit consists of a 737.5 μF capacitor bank with maximum voltage of 5.2 kV, which gives around 10 kJ maximum energy as described in [11]. In the current set up, the circuit gives maximum current of around *2 kA*. The fault current can be varied in two ways: by changing the voltage magnitude (V_{dc}) and by changing the trip signal delay (S signal).

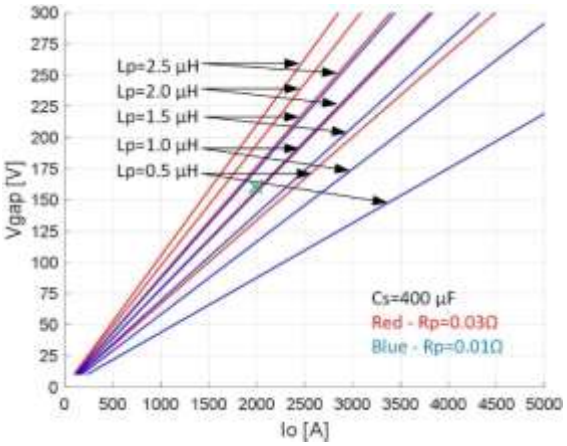

Fig. 3 Arc voltage vs commutating current with 400 μF capacitor.

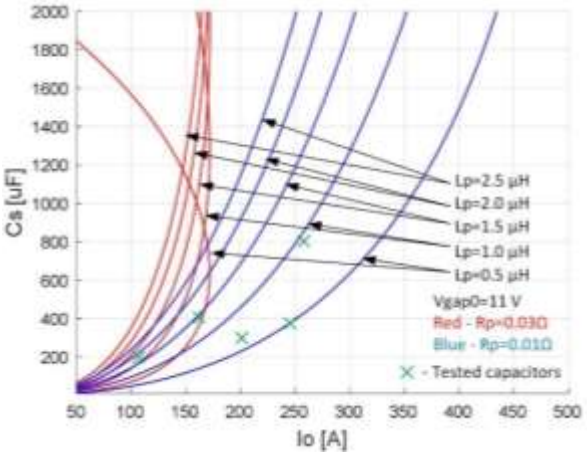

Fig. 4 Capacitance Cs versus I_0 with single break point (V_{gap0}=11 V).

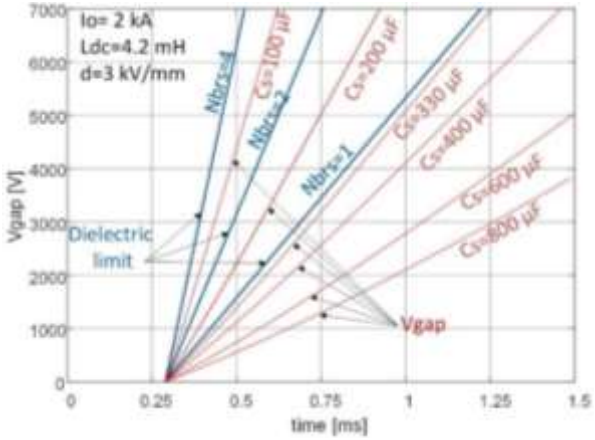

Fig. 5 Simulation of post-commutation gap voltage depending on capacitance.

B. Test DC CB

1) Circuit description

Fig. 6 shows photograph of the test DC CB. It includes UFD (S), capacitors (C_s) and arresters (SA). Residual switch (S_{res}) is not used in this study. The capacitor C_s is connected with UFD using *20×2* mm bus bars in order to reduce parasitic inductances. The location of current probes is also indicated.

2) Contact assembly

The contact assembly is detachable from the moving rods and has been modified from the UFD design in [11]. The first contact assembly is made with 2 break points as shown in Fig. 7. This assembly is used for tests with 1 break point, 2 break points in series and 2 break points in parallel. The upper contact is firmly connected to the dielectric holder. The lower contacts are approximately *20×10×8* mm and they are supported by springs and guiding pins in order to provide contact force in the closed state. The contact surface in closed state is around *40 mm²* on each break point (depends on the exact overlap OL).

Fig. 6 LC DC Circuit Breaker.

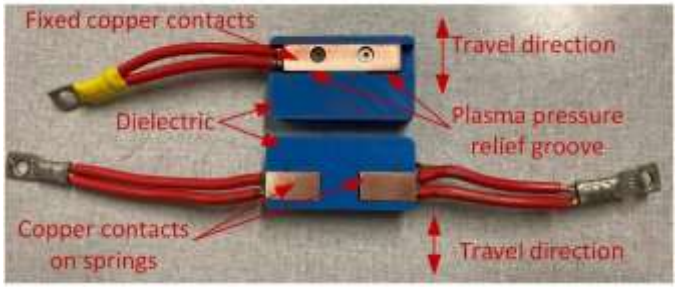

Fig. 7 Contact assembly used for 1 and 2 series/parallel break points.

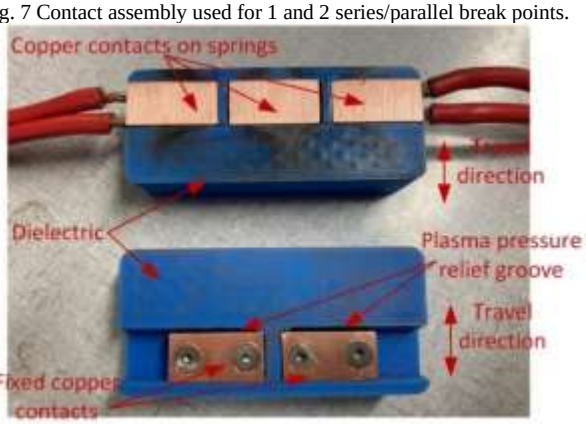

Fig. 8 Photograph of 4-break contact assembly.

Copper is chosen as the contact material because of manufacturing ease. Grooves are made in the dielectric along the contact leading edge in order to relieve plasma arc pressure. Two cables are used with each contact to provide adequate cross section and lower parasitics. The second contact assembly employs 4 break points as shown in Fig. 8. This design is chosen for simplicity to align the leading edge of all the contacts at *90°* to the travel axis to enable simultaneous separation at all breaking points. There are 3 contacts on springs and 2 fixed contacts. The contact surface is around *18 mm²* on each breaking point. The maximum gap distance is *3 mm* on each breaking point.

3) Capacitors C_s

Four different capacitors are evaluated as shown in Fig. 9, while technical details of the capacitors are given in Table II. Two units are available for each capacitor, and this enables experimentation with different capacitance and voltage levels, by using series or parallel connection. Different types of capacitors are not mixed in the circuit.

TABLE II DETAILS OF THE CAPACITORS TESTED IN THE DC CB.

Rating	Manufacturer	Dimensions (w×d×h) [mm]	Weight [kg]
400 µF, 6.5 kV	Gener. Atomics	360×183×278	23.2
300 µF, 10 kV	Vishay	245×350×657	68
2100 µF, 0.9kV	KEMET	Ø118×273	3.3
390 µF, 2.0kV	Vishay	Ø115×235	2.8

Fig. 9 Four capacitors tested with LC DC CB.

4) Arresters SA

The arresters are from EPCOS supplier, multiple metal-oxide B40 and B60 series basic units, and they are changed for each different capacitor. Their clipping voltage is selected to be just below the capacitor voltage rating, and below 6 kV. The required SA energy is estimated using PSCAD simulation, and the corresponding number of arrester units are paralleled.

C. Study methodology

The objectives of the study are to understand the commutation process, to evaluate the analytical model from

Section II. and dependencies on various parameters. The circuit in Fig. 6 is subjected to repeated tests with increasing current I_o and it is recorded if breaking is successful or not. However, the experimental circuit in Fig. 6 is not convenient for qualitative studies, since each unsuccessful case results in explosive, long arcing which destroys the copper contacts. This circuit is used for final confirmation of LC DC CB operation.

Another test circuit, as shown in Fig. 10, is used for qualitative studies and comparisons. It includes a transistor T_1 in series with UFD which serves as a back-up for current interruption. Arrester SA_{T1} is rated for 450 V (IGBT is rated for 1700 V) which is adequate for commutating well over 2 kA current, since the required commutating voltage is around 150 V according to Fig. 3. IGBT T_1 is commanded to open around *150 μs* after the expected arc-based commutation process. If arc commutation fails, then commutation is achieved with T_1 and circuit operates as DC CB with parallel capacitor described in [11]. This enables us to observe all the variables in the unsuccessful arc-based commutation transient in numerous tests, without destroying the contacts.

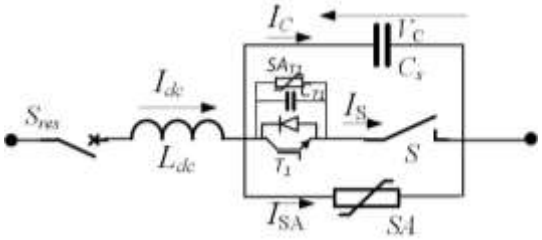

Fig. 10 Test LC DC Circuit Breaker with back-up commutating IGBT.

IV. Analysis of Multiple Break Points

A. *Break points connected in series*

There is abundant literature on arc voltage studies, both at low voltage [16] and high voltage [17],[18] applications. However, the commercial switches predominantly utilise single break point, while non-arcing disconnectors may employ multiple break points [14].

Fig. 11 shows I_s and I_c for 1,2 and 4 break points, for two different I_o current magnitudes: a) 600 A and b) 900 A. When contacts separate, arc voltage is developed which enables current commutation from S branch to C_s branch. If capacitor current I_c reaches the value of the fault current at separation (I_o), then switch current I_s is brought to zero and arc is interrupted. The peak I_{cp} of the capacitor current depends on the arc voltage V_{gap}, capacitance C_s but also on the parasitics in the commutating branch according to (2) [13]. This figure shows unsuccessful commutation, but it enables comparison of the peak capacitor current I_{cp}, which is expected to indicate the value of the fault current that can be interrupted.

It is seen that 2 break points increase commutating current almost twice compared with the single break, and similarly 4 break points further increase I_{cp}. The conclusion is that it is better to use multiple breaks with shorter arcs since larger current can be commutated, compared with a single long arc. This result validates the assumption with N_{brs} in the basic commutation model in (2) and in Fig. 2 and Fig. 3. The conclusions are valid at different currents in Fig. 11 a) and b).

Fig. 12 shows the measured arc voltages for the 900 A case in Fig. 11b). In the case of single break, it is visible that the electrode fall (the initial voltage) is around 11 V and the arc voltage increases as the gap distance is increasing which broadly agrees with the previous studies [15]-[18]. Arc voltage is not significantly dependent on the current magnitude, and this is the reason why I_{cp} has similar values at different I_o in Fig. 11.

With 2 break points we can observe two identical steps for the arc voltage which confirms the assumptions with V_{gap0} in Sections II. D. and II. E. The delay in the arc voltage steps is a result of free play and inaccuracies in the contacts assembly, occurring because of the limited manufacturing precision in the University workshop. It is seen that the peak current with two break points is *330A*, which is approximately *8.3%* lower than the current expected with simultaneous separation, i.e. two times larger than single break (*2×180A*). The corresponding angle on the L_pC_s cycle (T_p*=140 μs*) is obtained as $\alpha=38^o$, and according to (4) we can calculate that this delay causes *11%* lower peak current magnitude, which is broadly in agreement with the above experimental measurements.

In the case of 4 breaks, we can see 4 steps in the *30 μs* interval in Fig. 12. It is seen that each break point equally increases both: the electrode fall, and the slope of the arc voltage. The observed current peak is around *600 A*, which is *17%* lower than if all 4 breaks were separating simultaneously (*4×180 A = 720 A)*.

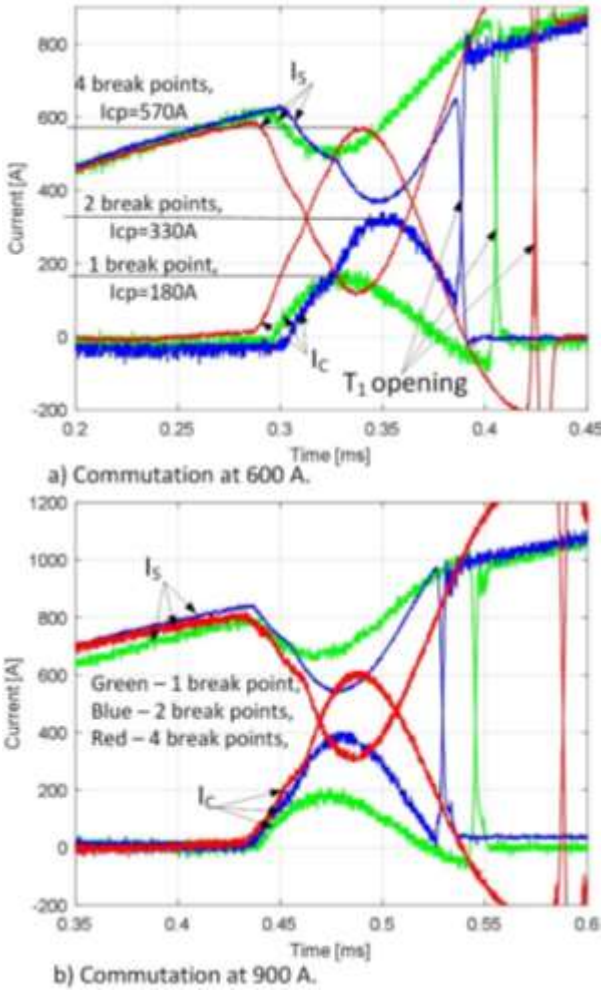

Fig. 11 Commutation of two different currents, with DC CB using different number of break points (400 μF, 6.5kV capacitor).

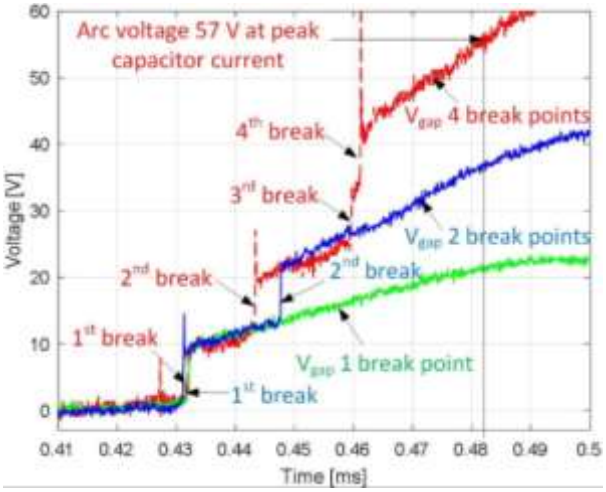

Fig. 12 Measured arc voltage (V_{gap}) for 1,2 and 4-break commutation at 900 A (400 µF, 6. 5kV capacitor).

Fig. 13 illustrates a 4-break commutation test with badly aligned contacts, which is shown here to enhance depth of commutation analysis. In this test the four break points separate within *130 µs*. It can be noticed that only the first 2 break points contribute to increasing I_c in the first peak I_{cp}, while the 3rd and the 4th break contribute to the irrelevant subsequent pulses.

B. *Parallel connection of break points*

Connecting break points in parallel benefits in lowering of current on each break point, and Fig. 14 shows the test circuit. Theoretically, according to (1) and (2), the effect of series and parallel connection should be the same. However parallel connection requires separate capacitors which in our case does not bring obvious benefit, as all capacitors can carry the rated commutating current in the short breaking interval. The designers of LC DC CB may be interested in parallel connection in case of applications with very high currents.

If one break point separates earlier, then the challenge is to prevent current transferring to the parallel branch with the second break. This is resolved by adding splitting inductors $L_1=L_2=200\ \mu H$ which are designed to prevent large current swings in *30-50 µs* commutating period.

Fig. 15 shows the experimental confirmation of operation in parallel topology. It is seen that cumulative effect ($I_{s1}+I_{s2}$) is similar as in the case of 2 break points in series in Fig. 11.

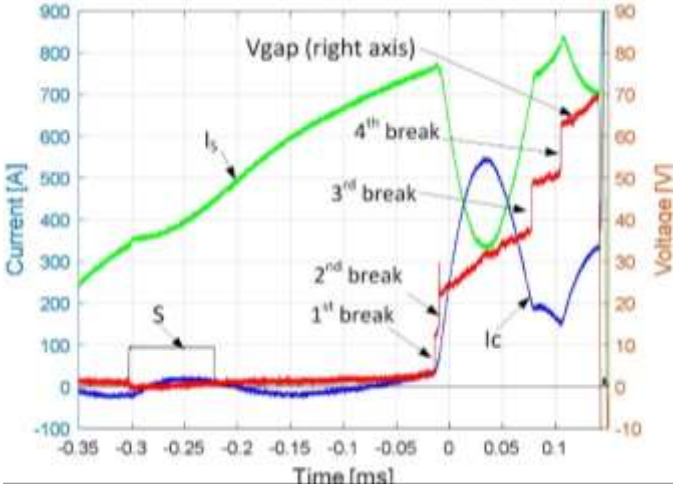

Fig. 13 Commutation with badly aligned contacts (800 µF, 6.5kV capacitor, 4 break points).

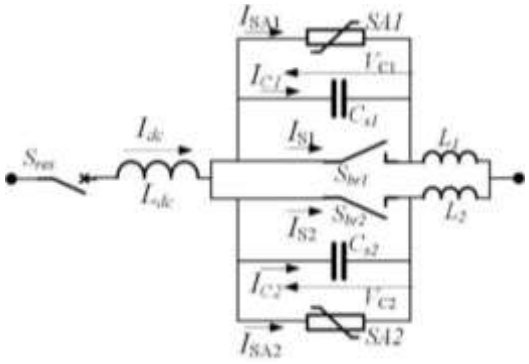

Fig. 14 LC DC Circuit Breaker with 2 parallel break points.

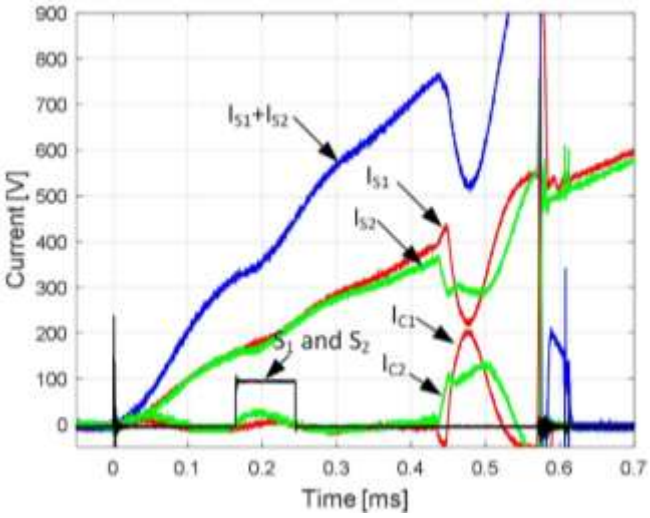

Fig. 15 Commutation with 2 parallel break points.

V. Analysis of Different Capacitors

All 4 capacitors from Fig. 9 are tested in LC DC CB, along with some further series/parallel connections. The aim is to evaluate I_{cp} with each capacitor, and to estimate parasitics L_{pc} and R_{pc} from Fig. 2. Fig. 16 shows the commutating current for 6 different capacitors, under the same conditions of around $I_o=900\ A$, with a single break. Although larger capacitance generally increases I_{cp}, the relationship is not simple or linear, and the measured I_{cp} is in general agreement with Fig. 4. As an example, *300 µF, 10 kV* capacitor gives higher commutating current than a larger *400 µF, 6.5 kV* capacitor. This is attributed to lower parasitic parameters. The model in (2) generally gives conservative values for I_{cp}. As capacitance increases, the model error is larger, and it grossly underestimates (by 20%) *580 A* commutation with *2100 µF, 0.9 kV* capacitor. This is attributed to the arc voltage dependence on the gap distance and current, and also dependence of the parasitics on the current and current derivative (frequency). The corresponding values for the 5 capacitors are marked with green crosses in Fig. 3 and Fig. 4.

The values for I_{cp} and half the damped oscillating period from Fig. 16 are recorded for each capacitor and used to estimate parasitics L_p and R_p. An iterative program with 2 unknowns is developed based on (2), and the calculated L_p and R_p are shown in Table III. These parameters are of high importance in the detailed non-linear models like LC DC CB model in [13] or arc model in [15]. Some of the tested capacitors have datasheets with manufacturer's parasitic parameters, but they are found to be significantly lower than the measured values in Table III.

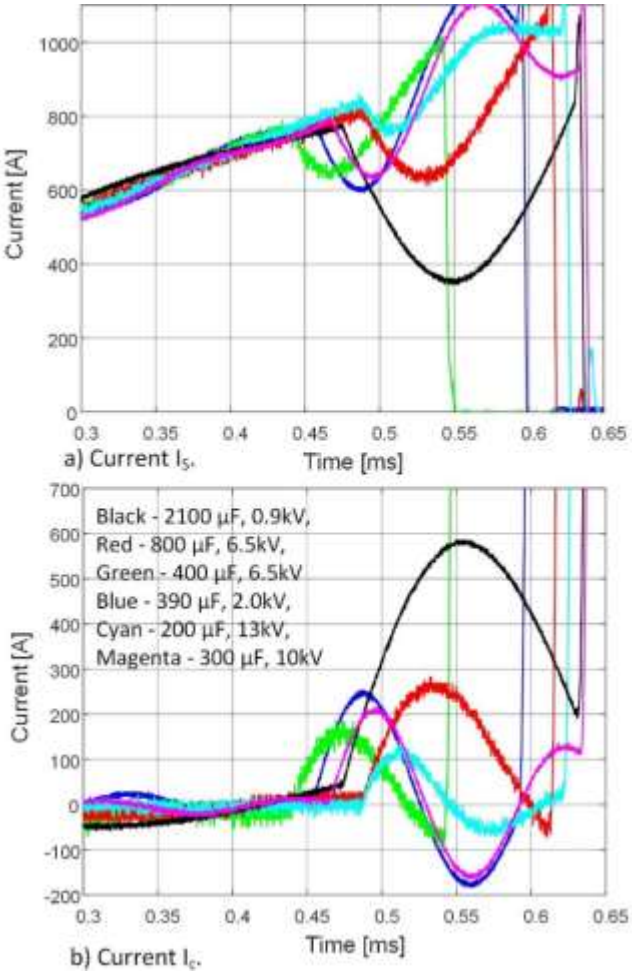

Fig. 16 Commutation at around 900 A for 6 different capacitors (1 break point).

TABLE III IDENTIFIED PARASITIC PARAMETERS.

Rating	Parasitic induct. L_p [µH]	Parasitic resis. R_p [mΩ]	Required no of break points $N_{brs,}$ for Io=2kA
400 µF, 6.5 kV	1.22	0.019	13
300 µF, 10 kV	1.42	0.008	10
2100 µF, 0.9kV	1.23	0.006	4
390 µF, 2.0kV	1.28	0.007	8

Using the I_{cp} values, and the model in (2), the number of series break points N_{brs} for a 2 kA DC CB can be estimated for each capacitor, as shown the last column in Table III. It is evident that there is a tradeoff between C_s and number of break points.

The responses in Fig. 16 enable further analysis of the impact of capacitor voltage rating, which is of high significance for developing LC DC CB module. Capacitor units of higher voltage rating will normally have higher parasitics, but tests conclude that this aspect does not have much impact on I_{cp}. The capacitor *390 µF, 2.0kV* has marginally better response than similar higher voltage capacitor (*400 µF, 6.5 kV* capacitor).

Fig. 17 shows comparatively I_{cp} values for one capacitor, at 4 different I_o values. The conclusion is that I_{cp} is practically independent of the magnitude of commutating current, which helps to simplify the study and reduce the number of tests. This conclusion may not apply at much higher current magnitudes and with a different insulating medium.

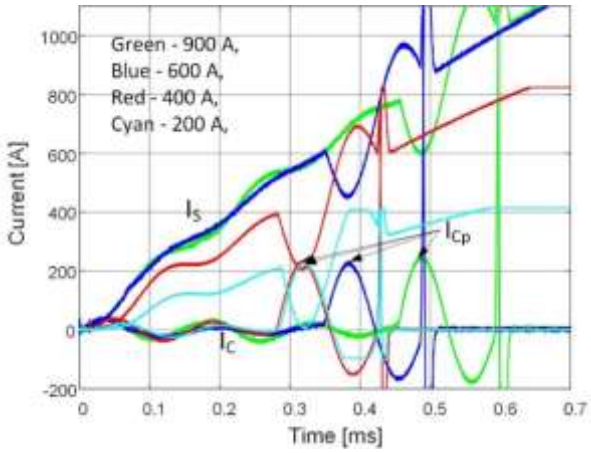

Fig. 17 Commutation at 4 different current values with the same capacitor (390 µF, 2.0 kV capacitor, 1 break point).

VI. COMPARISON OF DC CURRENT BREAKING RESULTS

A. Summary of tests

The conclusions form Sections IV. and V. are finally verified by testing on the circuit without IGBT T_1, from Fig. 6. Table IV summarizes the results, and shows the largest DC current in the successful breaking tests for each topology. Not all topologies are tested, and the tested topologies are not always carefully evaluated in small steps, because of excessive number of required tests. The values obtained confirm conclusions related to the impact of breaking points and the capacitance and generally align with the current values obtained in the studies with I_{cp}. The peak capacitor current I_{cp} obtained as described in this article (either experimentally or using the model) is a good indicator of the maximum current I_o that can be commutated.

With parallel connection, only *400 µF, 6.5 kV* capacitor is tested, and *260 A* (130 A per break point) is successfully commutated, which is similar as with 2 break points in series.

B. Illustration of successful breaking

Fig. 18, shows the recording for one of the cases from Table IV, with *800 µF, 6.5kV* capacitor and 4 break points. It shows that *930 A* is commutated *290 µs* after the trip signal, and breaker voltage rises to *4.3 kV* in *2.5 ms*. The result also demonstrates feasibility of rising voltage stress while disconnector contacts are moving, as analysed in Fig. 5.

Fig. 19 shows the successful interruption of *1530 A* with *2100 µF, 0.9 kV* capacitor, which may not have high significance for practical application because of the low voltage rating. Also, this capacitor would violate the condition in (5) leading to slow DC CB. Nevertheless, this case is shown for completeness, and it demonstrates that the core principle of LC DC CB operates successfully for high currents. Inspection of the arc voltage curve reveals that this topology could potentially break higher current. It is seen that the gap voltage equals arc voltage of around *53 V* just before the end of commutation and then it drops to the circuit voltage of *40 V* when arc is extinguished. This voltage step at the end of commutation represents margin for successful commutation. Unfortunately, this topology has not been tested at higher currents. These two figures also show that the arcing (commutation) interval is very short, i.e. around *50 µs* in Fig. 18 and *70 µs* in Fig. 19. The

duration of commutation is determined by the delay between breaking points. If these delays are eliminated (better alignment of contacts), then duration of commutation would be limited by ¼ of C_sL_p cycle, which is *30-50 µs.* The average time to contact separation (T_o*=290 µs*) is constant although there is randomness in the separation time for the individual break points between tests.

C. Impact of thermal phenomena

It is confirmed that LC DC CB successfully breaks all current values below the values in Table IV. In general, the authors have not observed randomness or stochastic phenomena in the results. This is attributed to extremely short arcing which eliminates thermal phenomena (arcing lasts up to *70 µs* for successful breaking). Fig. 20 shows photograph of contacts after around *100* tests. The arcing points are visible, but the contacts operate well, and it is concluded that the damage is not severe, although contact lifetime has not been tested.

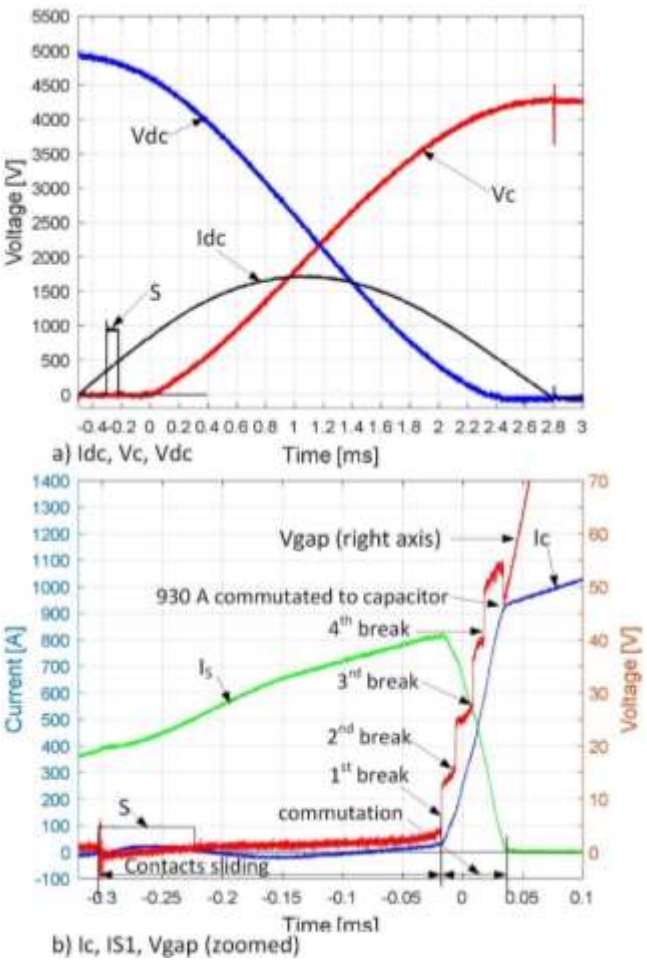

Fig. 18 Successful commutation of 930 A. 4 break points, 800 µF, 6.5 kV C_s.

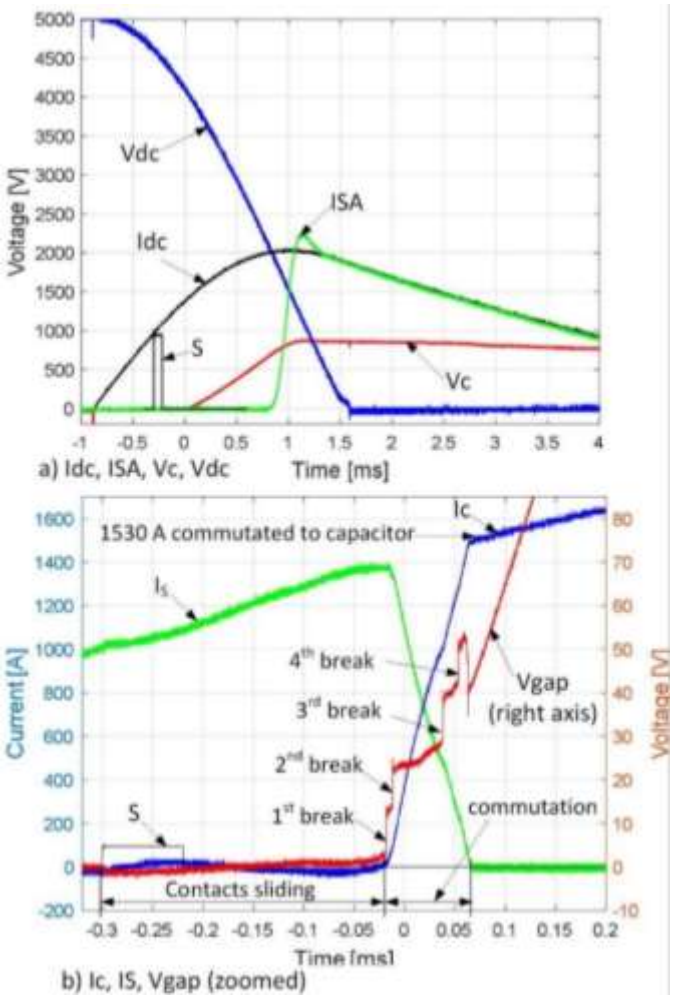

Fig. 19 Successful breaking of 1530 A. 4 break points, 2.1 mF, 0.9 kV capacitor.

TABLE IV RECORD OF SUCCESSFUL TESTS SHOWING MAXIMUM COMMUTATING CURRENT.

Capacitors		One capacitor	2 in parallel	2 in series
400 µF, 6.5 kV	1 break point	400 µF, 6.5 kV, 170 A	800 µF, 6.5 kV, 285 A	200 µF, 13 kV, 150 A
	2 break points	400 µF, 6.5 kV, 295 A	800 µF, 6.5 kV, 530 A	-
	4 break points	-	800 µF, 6.5 kV, 930 A	-
300 µF, 10 kV	1 break point	300 µF, 10 kV, 190 A	-	-
	2 break points	300 µF, 10 kV, 350 A	-	-
	4 break points	300 µF, 10 kV, 530 A	-	-
2100 µF, 0.9kV	1 break point	2100 µF, 0.9 kV, 490 A	-	-
	2 break points	-	4200 µF, 0.9kV 1680 A	1050 µF, 1.8kV, 550 A
	4 break points	2100 µF, 0.9 kV, 1530 A	-	-
390 µF, 2.0kV	1 break point	390 µF, 2.0kV, 200 A	-	-
	2 break points	-	-	-
	4 break points	-	780 µF, 2.0kV, 1050 A	-

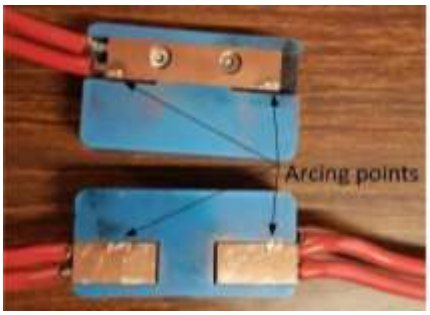

Fig. 20 2-break contacts after around 100 tests.

VII. Development of Module and High-Voltage Unit

A. Upscaling principles

These studies indicate that multiple series break points are particularly beneficial for developing LC DC CB technology. They enable using lower capacitance or lower speed UFD, and they provide higher arc voltage which facilitates commutating larger currents according to (1) and (3). On the downside, higher number of contacts increases weight of the moving mass of UFD and require good manufacturing precision. It is not clear where would be manufacturing limits on the number of break points, but the commercial UFD reported in [14] shows 14 break points, arranged as 2 rows of 7 breaks in series.

With the view of HV DC transmission application, we would expect that commutating current I_o will be only *4-6 kA*, since this DC CB topology commutates current within short interval after the trip signal (T_o). Assuming that 10 break points is feasible, then the required capacitance will be of the order of *400-800 µF*, and it would also satisfy voltage rise condition (5).

The capacitor value of *400-800 µF* is too large for a single unit at transmission voltages. Modular design will be needed with module voltage predicted in the range *5-20 kV*. Capacitors will facilitate good voltage sharing for series connection.

The initial arc voltage in our tests is 11 V which is at the lower end of the values reported with tests on commercial switches [16][18]. This voltage potentially could be increased with improved contact geometry and material, or dielectric.

B. Test case comparison with current injection DC CB

The LC DC CB with 300 µF, 10 kV, 530 A case from Table IV is considered for upscaling. Conservatively assuming the same switch with 4 break points, and using four parallel capacitors, an LC DC CB module of 10 kV, 1.2 mF, and with 2120 A commutating capability will be obtained. Connecting six modules in series will give 60 kV, 200 µF, 2120 A unit.

The basic 40 kV, 9 kA, 3 ms (60 kV peak voltage) current injection DC CB unit employed in Nan'Ao project as described in [6] is used for comparison.

The test circuit with firm *40 kV DC* voltage source and a series inductor L_{dc}*=16 mH* is adopted for comparing the two DC CBs. The initial load current of 1 kA is adopted. The trip signal is sent 170 µs after the fault (protection detection time) for both DC CBs and current value at trip signal is 1.425 kA. Table V shows all calculated parameters and performance indicators obtained using PSCAD simulation for the two topologies.

Fig. 21 shows comparatively PSCAD simulation of DC fault clearing with the two DC CB topologies. The key advantage of LC DC CB is earlier commutation, and this results in peak line current of only 54%, and the dissipated energy is 30% of the energy with the current injection DC CB. The current at commutation is also lower and current reaches peak earlier.

Comparing the components, the capacitor C_s is 20 times larger with LC DC CB. However, LC DC CB uses only one switch (consisting of 6 units in series) while current injection DC CB needs 3 and an additional inductor L_s. It is seen in Fig. 21a) that the gap voltage reaches peak value in approximately the same time (3 ms), which means LC DC CB disconnector speed is not well utilised (because of large C_s).

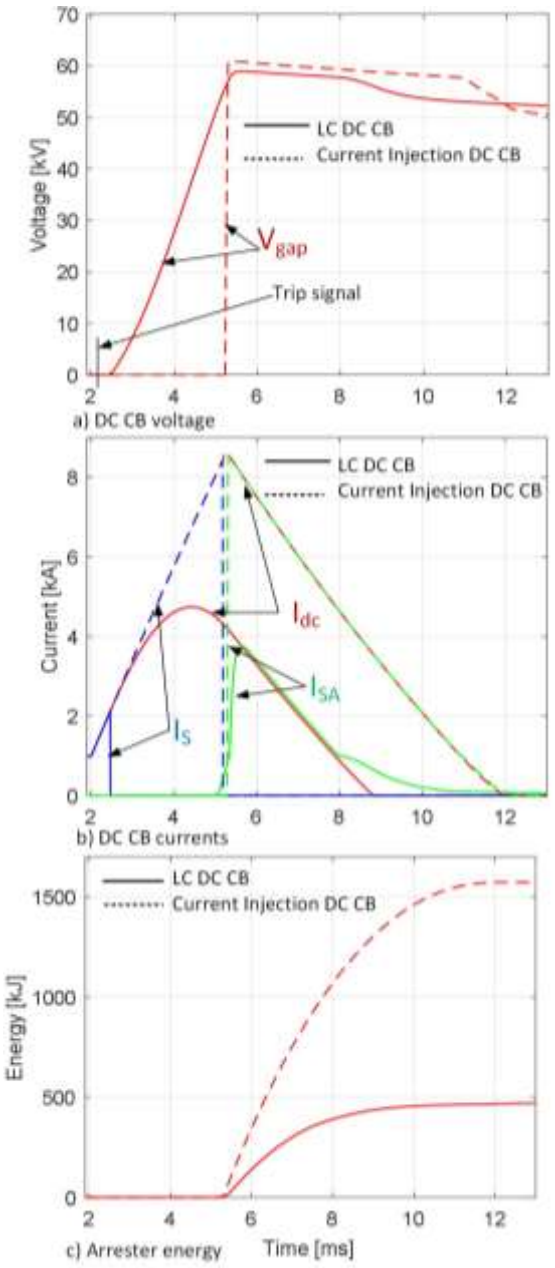

Fig. 21 Comparison by simulation of LC DC CB and current injection DC CB.

TABLE V PARAMETERS OF LC AND CURRENT INJECTION DC CB.

Parameter	LC DC CB	Current Injection DC CB
L_{dc}	16 mH	16 mH
L_s	-	0.4 mH
C_s	200 µF, 60 kV	10 µF, 60 kV
S	Disconnector, 3 ms	Vacuum interrupter, 3 ms
S_2	-	Vacuum interrupter, 3 ms
V_{dc}	40 kV	40 kV
V_{dccb}	61 kV	59 kV
I_{cp}	2.1 kA	8.5 kA
I_{dcp}	4.7 kA	8.7 kA
E_{arr}	472 kJ	1573 kJ
Commutation	0.29 ms	3 ms

VIII. CONCLUSION

The article presents analysis of design options for a practical *2- 10 kV, 2 kA* LC DC Circuit Breaker module. The principal conclusion is that disconnectors with multiple break points significantly contribute to increase commutating current and reduce the size of capacitor. The experimental tests with *5 kV* ultrafast disconnector demonstrate that arc voltage increase proportionally with each breaking point. Further modeling and testing with different capacitors concludes that larger capacitances increase commutating current, but relationship is complex and non-linear. Successful breaking is demonstrated on hardware in the laboratory for multiple cases including: *930 A* with *800 µF, 6.5 kV*, capacitor, 530 A with *300 µF, 10 kV*, capacitor and *1530 A* with *2100 µF, 0.9 kV*, capacitor.

It is recommended that the LC DC CB module design should firstly consider maximizing the number of break points in series. Assuming around 10 break points, the required capacitance will be of the order of *400-800 µF* for commutating 4-6 kA currents. The module voltage is expected to be 5-20 kV. The comparison with current injection DC CB reveals advantages in lower peak current and dissipated energy.

IX. ACKNOWLEDGMENT

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XI. BIOGRAPHY

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