

Analysing Flow Security Properties in Virtualised Computing Systems

Chunyan Mu

Department of Computer Science, Teesside University, U.K.
c.mu@tees.ac.uk

Abstract. This paper studies the problem of reasoning about flow security properties in virtualised computing networks with mobility from perspective of formal language. We propose a distributed process algebra CSP_{4v} with security labelled processes for the purpose of formal modelling of virtualised computing systems. Specifically, information leakage can come from observations on process executions, communications and from cache side channels in the virtualised environment. We describe a cache flow policy to identify such flows. A type system of the language is presented to enforce the flow policy and control the leakage introduced by observing behaviours of communicating processes and behaviours of virtual machine (VM) instances during accessing shared memory cache.

Keywords: information flow control, language-based security, cache non-interference, virtualised computing systems.

1 Introduction

Cloud computing has attracted interests in both the scientific and the industrial computing communities due to its ability to provide flexible, configurable, and cost-effective computing resources delivered over the internet. In cloud systems, computing resources are shared among multiple clients. This is achieved by virtualisation in which a collection of virtual machines (VMs) are running upon the same platform under the management of the hypervisor. Virtualisation allows computing service providers to maximise the utilisation of the devices and minimise the costs by creating multiple VMs over a shared physical infrastructure. However, such services can also bring additional channel threat, and introduce information leakage between unrelated entities during the procedure of *resource sharing* and *communications* through unintended covert channels. To address this concern, this paper proposes to develop formal approaches to specifying, modelling and analysing flow security properties in virtualised computing networks, which are the key underpin of contemporary society such as cloud computing.

Specifically, information leakage can come from observations on both program executions and cache usage in the virtualised environment. On the one

hand, for processes running upon a particular VM instance, consider the processes are communication channels, sensitive inputs can be partially induced by observing public outputs of the processes regarding choices of public inputs. On the other hand, shared caches enable competing VM instances to extract sensitive information from each other. CPU cache, a small section of memory built in the CPU for fast memory access, is one of the highest-rate measurable resources shared by multiple processes [32]. Therefore cache-based side-channel attack becomes one of the major attack on VMs and receives the most attention in the cloud environment [24]. Consider a malicious VM repeatedly access shared cache memory to perform cache-based side-channel attacks. Such attacks allow one virtual machine to effectively steal secrets of another hosted machine in the same cloud environment. More precisely, for processes running upon different VM instances, cache usage can be considered as a communication channel. Consider the cache lines accessed by the victim instance and by the malicious instance as high level input and low level input respectively, by observing the usage (such as time) of victim cache lines (low output), the malicious observer can learn some information of the victim instance. In summary, this paper considers distributed virtualised computing environment where the attacker VM steals the information from the target one by observing executions of victim processes, and by probing and measuring the usage (timing) of the shared cache.

In particular, we develop an approach from the software language-based level to enforce the applications to access shared cache and to bring interferences in a predictable way. As a result, we aim to prevent the leakage introduced by such cache timing channel and the interference between security objects caused by executions. First, we propose a CSP-like language for modelling communicating processes running upon VMs with mobility in the computing environment. Second, we formalise a cache flow policy to specify the security condition regarding the threat model we focus on. Finally, we describe a type system of the language to enforce the flow policy and control the leakage introduced by observing the system behaviours. More specifically, we give an identifying label to each VM instance, and partition the cache into a set of page-sized blocks, each block in pages is mapped to a set of cache lines and is dynamically granted the label of its owner (the VM instance it is allocated to). The label of the block will be revoked when its owner terminates. In addition, programming variables and cache lines are assigned security labels to denote the security levels of the data they store. VM instances and hosts are assigned to different categories for the purpose of controlling information flow introduced by processes and VM instances movements. When a guest VM is launched, the VM manager allocates cache pages to it regarding its requests. During the running time of the VM process, operation of cache lines is allowed only if it satisfies the specified flow policy. Processes are allowed to move from one VM to another, and VM instances are allowed to move from one host to another. However, movements from a lower-ordered category carrier to a higher one are not allowed. Furthermore, we only allow the communicating process access the cache within a certain time in order to prevent timing leaks by observing the usage of the cache. These regulations are

enforced by the semantics and the typing rules we formalised. When the guest VM terminates, the relevant cache pages are initialised, and released to the VM manager to prevent flushing of the pages by a malicious VM.

Outline. This paper is organised as follows. Section 2 describes our language for modelling basic virtualised computing networks. Section 3 describes the threat model we focus on. Section 4 specifies cache flow policy which the processes should satisfy in our model. Section 5 presents a type system to enforce the cache flow policy. Section 6 briefly reviews literature in the related areas.

2 The Modelling Language CSP_{4v}

This section presents a dialect of communicating sequential processes (CSP) [10] language CSP_{4v} for formal modelling of and reasoning about virtualised computing network systems considered in this paper. Such an environment can be considered as a distributed computing system, in which a group of inter-connected and virtualised computers are dynamically allocated for serving. Processes can move from one VM to another and communicate to each other via sending/receiving messages. Applications and data are stored and processed in the network but can be accessed from any location using a client. It is natural to specify and describe the system as a set of communicating processes in a network with consideration of resource sharing in a predictable way. A CSP-like language is therefore a good choice for modelling of such systems.

2.1 Terminology and notation

We consider the infrastructure consists of a set of *virtual private networks* (VPNs) upon which a set of *virtual machines* (VMs) can communicate with each other. A VPN may include one or more VMs, and the location of VMs can be viewed as a node (host) of the VPN it belongs to. An *instance* is a VM upon which a number of *processes* locate and run. Let I denote a set of instances, $I = \{I, I_1, \dots, I_n\}$. Processes (P, P_1, \dots) can be constructed from a set of atomic actions called *events* (e, e_1, \dots) , or be composed using operators to create more complex behaviours. The full set of actions that a system may perform is called the *alphabet* (Σ) . The operators are required to obey algebraic laws which can be used for formal reasoning. The interactions carrying data values between processes take place through “channels”. From an information theory point of view, a storage device such as cache which can be received from (reading) and sent to (writing) is also a kind of communication channel. CPU data caches locate between the processor cores and the main memory. We assume the clients (including the attacker) know the map between memory locations and cache sets, so we omit the details of the mapping and focus on cache organisation and operation here. Cache can be viewed as a set of cache lines: $\text{CLines} = \{l_i | 0 \leq i \leq n\}$ where n denotes the size of the cache.

In addition, in order to encode the desired features of the language for flow secure virtualised computing systems, we assign security labels into variables and cache lines (channels), and allocate cache lines into instances via mappings:

$$\tau_v : \mathbf{Vars} \mapsto_{\tau_v} \mathbf{L}, \quad \tau_c : \mathbf{CLines} \mapsto_{\tau_c} \mathbf{L}, \quad \alpha_c : \mathbf{CLines} \mapsto_{\alpha_c} I$$

where \mathbf{L} denotes a security lattice. We write τ instead of τ_v and τ_c in general for cases without introducing any confusion. Furthermore, we consider VM hosts are assigned to different categories Ω_H , with an ordering of subset relations:

$$\beta_h : \mathbf{Hosts} \mapsto_{\beta_h} \Omega_H.$$

For instance, h_1 is assigned to category: $\Omega_1 = \{\mathbf{student}\}$, h_2 is assigned to category: $\Omega_2 = \{\mathbf{student}, \mathbf{staff}\}$, and thus $h_1 \sqsubseteq h_2$ since $\Omega_1 \subseteq \Omega_2$. Similarly, we also assign VM instances into different sub-categories Ω_I , with an ordering of subset relations:

$$\beta_i : \mathbf{VMs} \mapsto_{\beta_i} \Omega_I.$$

For instance, P running upon VM i_1 belonging to sub-category: $\omega_1 = \{\mathbf{UG-1}\} \subseteq \mathbf{student}$, Q running upon VM i_2 belonging to sub-category: $\omega_2 = \{\mathbf{UG-1}, \mathbf{UG-2}\} \subseteq \mathbf{student}$, and $\omega_1 \subseteq \omega_2$, so $i_1 \sqsubseteq i_2$.

2.2 Syntax

Table 1 presents the syntax of the language \mathbf{CSP}_{4v} . Expressions can be vari-

| | |
|---------------------|---|
| Expressions | $\text{exp} ::= \mathbf{Vars} \mid \mathbf{CH} \mid \mathbf{INTS} \mid \text{exp} \oplus \text{exp} \quad (\oplus \in \{+, -, *, /\})$ |
| Boolean expressions | $b ::= \mathbf{true} \mid \neg b \mid b \wedge b \mid \text{exp} \bowtie \text{exp} \quad (\bowtie \in \{>, \geq, <, \leq, ==\})$ |
| Process | $x ::= \text{exp} \mid \mathbf{STOP} \mid \mathbf{SKIP} \mid \mathbf{SLEEP}(\Delta t) \mid$ $\quad \mathbf{MOVE}_P(i) \mid P; Q \mid P \triangleleft b \triangleright Q \mid b \triangleright (P)^* \mid$ $\quad a!w \mid a?x \mid P \parallel Q$ |
| VM instances | $I ::= \llbracket P \rrbracket \mid \mathbf{MOVE}_I(h) \mid I \parallel I'$ |
| Hosts | $H ::= i : \llbracket I \rrbracket.M_I \mid H \parallel H'$ |
| VPN networks | $G ::= h : \llbracket H \rrbracket \mid G \parallel G'$ |

Table 1. Syntax of \mathbf{CSP}_{4v}

ables, channels, integers and arithmetic operations (denoted by \oplus) between expressions.

Operator $x := \text{exp}$ assigns the value of exp to process variable x . Action operator \mathbf{STOP} denotes the inactive processes that does nothing and indicates a failure to terminate, and delayable operator $\mathbf{SLEEP}(\Delta t)$ allows the process to do nothing and wait for Δt time units. Moving operator $\mathbf{MOVE}_P(i)$ allows a process P to be able to move from current VM to another one i . We require that VM processes running upon on a VM instance with lower (category) order are not

allowed to move to a VM instance with a higher (category) order. Operator $P; Q$ denotes the sequential composition of processes P and Q . Branch operator $P \triangleleft b \triangleright Q$ defines if the boolean expression b is true then behaves like P otherwise behaves like Q . Sending operator $a!(w)$ will output a value in expression w over channel a to an agent, and receiving operator $a?x$ allows us to input a data value during an interaction over channel a and write it into variable x of an agent. $P \parallel Q$ denotes the synchronous parallel composition of processes P and Q . Loop operator $b \triangleright (P)^*$ denotes the loop operation of process P while b is true.

An instance I is a virtual machine (VM) hosted on a network infrastructure. Operator $\llbracket P \rrbracket$ defines the VM upon which process P runs. Operator $\text{MOVE}_I(h)$ allows VM instances (with all processes running on it) to migrate from current host machine to another host h to keep the instance running even when an event, such as infrastructure upgrade or hardware failure, occurs. Similarly to the process movement, we require that VM instances running upon on a host with lower (category) order are not allowed to move to a host with a higher (category) order. So, in the previous example, instances running upon h_1 are not allowed to moved to h_2 , and P is not allowed to move to VM i_2 . Operator $i : \llbracket I \rrbracket . M_I$ defines the host machine upon which I runs, M_I denotes the cache pages allocated to instance I . To ensure that no cache is shared among different VM instances, we require that for any host h upon which any I_1 and I_2 are running: $I_1 \neq I_2 \Rightarrow M_{I_1} \cap M_{I_2} = \emptyset$, and if an instance I terminates, then set M_I to be \emptyset for future allocation to other instances. Virtual private network provides connectivity for VM hosts. It can be viewed as a virtual network consisting of a set of hosts where VM instances can run and communicate with each other. The location of a host $h : \llbracket H \rrbracket$ indicates a network node of G in which the VM host machine locates.

2.3 Operational semantics

In order to incorporate as much parallel executions of events within different nodes as possible, we transform the network G into a finite parallel compositions of the form:

$$\begin{aligned} G = & h_1 : i_{11} : \llbracket P_{11} \rrbracket . M_{11} \parallel \dots \parallel h_1 : i_{1j_1} : \llbracket P_{1j_1} \rrbracket . M_{1j_1} \\ & \parallel h_2 : i_{21} : \llbracket P_{21} \rrbracket . M_{21} \parallel \dots \parallel h_2 : i_{2j_2} : \llbracket P_{2j_2} \rrbracket . M_{2j_2} \\ & \parallel \dots \dots \dots \\ & \parallel h_m : i_{m1} : \llbracket P_{m1} \rrbracket . M_{m1} \parallel \dots \parallel h_m : i_{mj_m} : \llbracket P_{mj_m} \rrbracket . M_{mj_m} \end{aligned}$$

where h_k denotes the identifier of a host, i_{kj} denotes the VM instance located at h_k . Each component $h_k : i_{kj} : \llbracket P_{kj} \rrbracket . M_{kj}$ is considered as a *decomposition* of G . We argue such decomposition is well-defined by applying the following rules

of structural equivalence:

$$\begin{aligned}
G \parallel G' &\equiv G' \parallel G \\
(G \parallel G') \parallel G'' &\equiv G \parallel (G' \parallel G'') \\
h : \llbracket I \parallel I' \rrbracket &\equiv h : \llbracket I' \parallel I \rrbracket \equiv h : \llbracket I \rrbracket \parallel h : \llbracket I' \rrbracket \\
h : \llbracket (I \parallel I') \parallel I'' \rrbracket &\equiv h : \llbracket I \parallel (I' \parallel I'') \rrbracket \\
i : \llbracket P \parallel P' \rrbracket . M_i &\equiv i : \llbracket P' \parallel P \rrbracket . M_i \equiv i : \llbracket P \rrbracket . M_i \parallel i : \llbracket P' \rrbracket . M_i \\
i : \llbracket (P \parallel P') \parallel P'' \rrbracket . M_i &\equiv i : \llbracket P \parallel (P' \parallel P'') \rrbracket . M_i
\end{aligned}$$

We now define the operational semantics of CSP_{4v} in terms of multiset labelled transition system $\langle \mathbf{\Gamma}, \Sigma, \Longrightarrow \rangle$, where:

- $\mathbf{\Gamma}$ is a vector of configurations of a VPN G regarding the vector of decomposition of G . A configuration Γ , regarding a single component (say process P) of the decompositions of G , is defined as a tuple (σ, δ, I, H) , where:
 - $\sigma : \text{Vars}_P \mapsto \text{INTS}$ denotes the store;
 - $\delta : \text{CAddr}_P \mapsto (\text{INTS} \cup \{\emptyset\})$ defines the possible world regarding cache;
 - I specifies the owner (the VM instance identifier) of process P ;
 - H specifies the host (location) of the VM instance of process P .
- Σ is a set of operating events which the processes can perform;
- $\Longrightarrow \subseteq \mathbf{\Gamma} \times \Sigma \times \mathbf{\Gamma}$ is the multiset transition relations: Σ denotes a vector of operating events for the vector of components.

The action rules of the operational semantics of CSP_{4v} is presented in Table 2. Notations \Rightarrow , \Leftarrow , \Downarrow denote cache addressing, cache allocation, and evaluation respectively. For instance, $\Gamma \vdash \text{exp} \Downarrow v$ means that under configuration Γ , exp evaluates to value v , $w \Leftarrow \text{CAddr}_a$ means the cache allocated for expression w locates at CAddr_a , and $a \Rightarrow \text{CAddr}_a$ means cache address of channel a is CAddr_a , notation CAddr_P is used to denote the cache addresses allocated for P .

Store is defined as a mapping from variables to values, i.e., $\sigma : \text{Vars} \mapsto \text{INTS}$. Cache is considered as a mapping from addresses (of cache lines) to integers (cached) or \emptyset (flushed), i.e., $\delta : \text{CAddr} \mapsto (\text{INTS} \cup \{\emptyset\})$.

Action rule of assignment $\langle x := \text{exp}, \Gamma \rangle$ updates the configuration such that the state of x is the value v of expression exp after the execution. Action rule of process moving operator $\text{MOVE}_P(i')$ updates the configuration such that the identifier of instance accommodating P turns to be i' after the execution of the process movement. Similar action rule is applied for VM instance movement from one host to another. Action rule of sending operator $a!(w)$ updates the configuration such that the value stored in cache address (CAddr_a) is v , if expression w evaluates to v under configuration before the execution and the address of cache allocated for communicating channel a (to store expression w) is CAddr_a . Rule of receiving operator $a?x$ updates the configuration such that the state of variable x is v , if the value stored in cache address CAddr_a of the communicating channel is v under the configuration before receiving the data. In the cross-VM communications over today's common virtualised platforms, the cache transmission scheme requires the sender and receiver could only communicate by interleaving

| | |
|------------|---|
| Store | $S ::= \{\} \mid \{\mathbf{Vars} \mapsto \text{INTS}\} \cup S$ |
| Cache | $M ::= \{\} \mid \{\mathbf{CAddr} \mapsto (\text{INTS} \cup \{\emptyset\})\} \cup M$ |
| Stop | $\langle \text{STOP}, \Gamma \rangle \longrightarrow \Gamma[\delta(\mathbf{CAddr}_P) = \emptyset]$ |
| Skip | $\langle \text{SKIP}, \Gamma \rangle \longrightarrow \Gamma$ |
| Sleep | $\frac{\Delta t > 0}{\langle \text{SLEEP}(\Delta t), \Gamma \rangle \longrightarrow \langle \text{SLEEP}(\Delta t - 1), \Gamma \rangle} \quad \frac{\Delta t = 0}{\langle \text{SLEEP}(\Delta t), \Gamma \rangle \longrightarrow \Gamma}$ |
| Assignment | $\frac{\Gamma \vdash \text{exp} \Downarrow v}{\langle x := \text{exp}, \Gamma \rangle \longrightarrow \Gamma[\sigma(x) = v]}$ |
| Move | $\frac{\Gamma \vdash I \Downarrow i}{\langle \text{MOVE}_P(i'), \Gamma \rangle \longrightarrow \Gamma[I = i']} \quad \frac{\Gamma \vdash H \Downarrow h}{\langle \text{MOVE}_I(h'), \Gamma \rangle \longrightarrow \Gamma[H = h']}$ |
| Seq | $\frac{\langle P, \Gamma \rangle \longrightarrow \langle P', \Gamma' \rangle}{\langle P; Q, \Gamma \rangle \longrightarrow \langle P'; Q, \Gamma' \rangle} \quad \frac{\langle P, \Gamma \rangle \longrightarrow \Gamma'}{\langle P; Q, \Gamma \rangle \longrightarrow \langle Q, \Gamma' \rangle}$ |
| Branch | $\frac{\Gamma \vdash b \Downarrow \text{true}}{\langle P \triangleleft b \triangleright Q, \Gamma \rangle \longrightarrow \langle P, \Gamma \rangle} \quad \frac{\Gamma \vdash b \Downarrow \text{false}}{\langle P \triangleleft b \triangleright Q, \Gamma \rangle \longrightarrow \langle Q, \Gamma \rangle}$ |
| Send | $\frac{\Gamma \vdash \sigma(w) \Downarrow v \quad w \Leftarrow \mathbf{CAddr}_a}{\langle a!(w), \Gamma \rangle \longrightarrow \Gamma[\delta(\mathbf{CAddr}_a) = v]}$ |
| Recv | $\frac{a \Rightarrow \mathbf{CAddr}_a \quad \Gamma \vdash \delta(\mathbf{CAddr}_a) \Downarrow v}{\langle a?x, \Gamma \rangle \longrightarrow \Gamma[\sigma(x) = v]}$ |
| Loop | $\langle b \triangleright (P)^*, \Gamma \rangle \longrightarrow \langle (P; b \triangleright (P)^*) \triangleleft b \triangleright \text{SKIP}, \Gamma \rangle$ |
| Parallel | $\frac{P \longrightarrow P'}{P \parallel Q \longrightarrow P' \parallel Q} \quad \frac{I \longrightarrow I'}{I \parallel I'' \longrightarrow I' \parallel I''} \quad \frac{H \longrightarrow H'}{H \parallel H'' \longrightarrow H' \parallel H''} \quad \frac{G \longrightarrow G'}{G \parallel G'' \longrightarrow G' \parallel G''}$ |

Table 2. Operational semantics of CSP_{4v}

their executions for security concerns. In order to capture timing behaviour of cache-related operations, we consider the cache-related operations, such as communicating, as time-sensitive behaviours whose lasting time is recorded. The events are therefore considered as either non-delayable (time-insensitive, time does not progress) actions or delayable (time-sensitive, involves passing of time Δt) behaviour. We use $\Delta t(e)$ to denote the time duration of event e lasting for.

The behaviour of a process component can now be viewed as a set of sequences of *timed runs*.

Definition 1 (Timed run). *A timed run of a component of G is a sequence of timed configuration event pairs leading to a final configuration:*

$$\lambda = \langle \Gamma_0, (e_0, \Delta t_0) \rangle \rightarrow \cdots \rightarrow \langle \Gamma_n, (e_n, \Delta t_n) \rangle \rightarrow \Gamma$$

where, Γ_0 and Γ denote the initial and final configuration respectively. $\forall i \in \{0, n\}$, e_i is an event will take place with passing time Δt_i under configuration Γ_i ; if $\Delta t_i = 0$, e_i is considered as an immediate event, if $\Delta t_i > 0$, e_i is considered as a time-sensitive event with lasting time Δt_i .

3 Attacker Model

We consider computing environment where malicious tenants can use observations on process executions and on the usage of shared cache to induce information about victim tenants. We assume the service provider and the applications running on the victim’s VM are trusted. Let us consider the attacker owns a VM and runs a program on the system, and the victim is a co-resident VM that shares the host machine with the attacker VM. In particular, there are two ways in which an attacker may learn secrets from a victim process: by probing the caches set and measuring the time to access the cache line (through the cache timing channel), and by observing how its own executions are influenced by the executions of victim processes.

Cache timing side channel (C1). In the virtualised computing environment, different VMs launch on the same CPU core, CPU cache can be shared between the malicious VM and the target ones. Consider the malicious VM program repeatedly accesses and monitors the shared cache to learn information about the sensitive input of the victim VM. Specifically, timings can be observed from caches and are the most common side channels through which the attacker can induce the sensitive information of the victim VM. Intuitively, such cache side channel can be viewed as a communication channel, the victim and the attacker can be viewed as the sender and the receiver respectively. We assume that the attacker knows the map between memory locations and cache sets, and is able to perform repeated measurements to record when the victim process accesses the target cache line. We focus on cache timing side channel, all other side-channels are outside our scope.

Example 1. Consider the scenario presented in Fig. 1, where VM_1 (victim VM, labelled i_1) and VM_2 (attacker VM, labelled i_2) be two instances running upon $Host_1$ (labelled h_1); victim processes P and Q , running over VM_1 , are communicating to each other: P generates a key and sends it to Q , Q encrypts a message using the received key and sends the encrypted message to P , P receives the message and decrypts it; and attacker process R , running over VM_2 , keeps probing cache address of the key. Let `keyGen`, `encrypt` and `decrypt` denote the function of generating a key, encryption and decryption respectively, and assume `cread(CAddr)` is a function probes cache address `CAddr`: returns 1 if it is available and returns -1 otherwise. We present the model in our language as

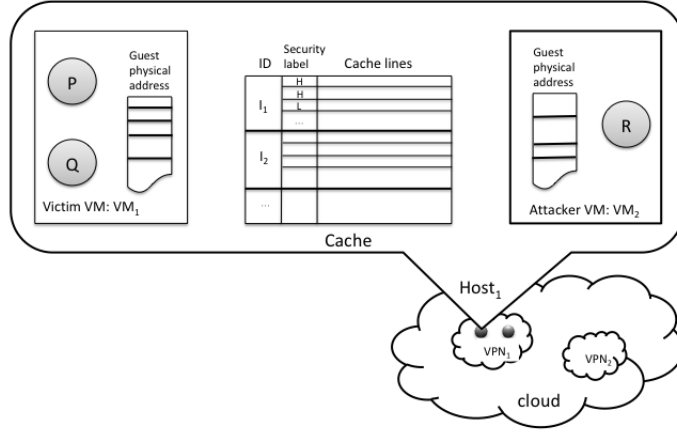


Fig. 1. Composition structure of the example in networks

follows.

$$\begin{aligned}
 VPC_1 &\stackrel{\text{df}}{=} h_1 : [\text{Host}_1] \parallel h_2 : [\text{Host}_2] \\
 \text{Host}_1 &\stackrel{\text{df}}{=} i_1 : [\text{VM}_1].M_{\text{VM}_1} \parallel i_2 : [\text{VM}_2].M_{\text{VM}_2} \\
 \text{VM}_1 &\stackrel{\text{df}}{=} [P \parallel Q] \quad \text{VM}_2 \stackrel{\text{df}}{=} [R] \\
 P &\stackrel{\text{df}}{=} x := \text{keyGen}(); \text{key!}x \rightarrow P' \\
 Q &\stackrel{\text{df}}{=} \text{key?}y \rightarrow Q' \\
 Q' &\stackrel{\text{df}}{=} m_1 := \text{encrypt}(y, \text{"message"}); \text{msg!}m_1 \rightarrow \text{STOP} \\
 P' &\stackrel{\text{df}}{=} \text{msg?}m_2 \rightarrow P'' \\
 P'' &\stackrel{\text{df}}{=} m := \text{decrypt}(x, m_2) \rightarrow \text{STOP} \\
 R &\stackrel{\text{df}}{=} \text{true} \triangleright (z := \text{cread}(\text{CAddr}_{\text{key}}))^*
 \end{aligned}$$

The communication time between P and Q is affected by the value of the key generated. There is information flow from victim VM to malicious VM through cache side channel.

Leakage through observations on process executions (C2). Next let us focus on processes running upon a particular VM instance. Consider the VM instance, upon which processes are running, as a communication channel having inputs and outputs, which is relative to information flow from victim user to a malicious one. The victim user controls a set of higher level inputs with confidential data.

The attacker is an observer who may have control of lower level inputs. He has partial observation on executions of the process, but does not have any access to the confidential data. Specifically, the weak attacker can observe the public result, i.e., the final public output of the programs, while the strong attacker can observe the low state after each execution step of the processes. We consider a process has access to confidential data via higher level inputs. The attacker tries to collect and deduce some of the secure information about higher level inputs by varying his inputs and observing the execution of the process.

Example 2. Consider process P and R are running upon a VM instance VM . Process P inputs a password through channel pwd into H -level variable x , and updates L -level variable y to be 1 if x is odd and to be 0 if x is even. Process R output variable y through channel res :

$$\begin{aligned} \text{VM} &\stackrel{\text{df}}{=} \llbracket P \parallel R \rrbracket \\ P &\stackrel{\text{df}}{=} \text{pwd}?x; \ y := 1 \triangleleft (x \bmod 2 == 1) \triangleright y := 0 \rightarrow \text{STOP} \\ R &\stackrel{\text{df}}{=} \text{res}!(y) \rightarrow \text{STOP} \end{aligned}$$

Assume $L \sqsubset H \in \mathbf{L}$. Clearly there are implicit flows from x to y by observing L -level output of the process.

4 Information Flow Policy

Information flow is controlled by means of security labels and flow policy integrated in the language. Each of the identifiers, information container, is associated with a security label. Identifiers can refer to variables, communication channels, and can refer to entities such as files, devices in a concrete level. The set of the security labels forms a security lattice regarding their ordering. We study the system flow policy which prevents information flow leakage from high-level objects to lower levels and from a target instance to a malicious one via observing process executions and cache usage (by measuring the time of accessing cache lines during communications).

In general, information flow policies are proposed to ensure that secret information does not influence publicly observable information. An ideal flow policy called Non-interference (NI) [8] is a guarantee that no information about the sensitive inputs can be obtained by observing a program's public outputs, for any choice of its public inputs. Intuitively, the NI policy requires that low security users should not be aware of the activity of high security users and thus not be able to deduce any information about the behaviours of the high users. On the one hand, for processes running upon a particular VM instance (regarding **C2**), the NI policy can be applied to control information flow from high-level input to low-level output, where state of sensitive information container (s.a. high-level variables) and observations on behaviours of public information container (s.a. low-level variables) are viewed as the high input and low output respectively. On the other hand, for processes running upon different VM instances (regarding **C1**), we adapt the NI policy here in order to control the information flow

from processes running upon victim instance to malicious one through cache side channel. Consider the cache side channel as a communication channel, the cache lines accessed by the victim instance and by the malicious instance are viewed as high level input and low level input respectively, and the observations on the victim cache usage (s.a. hits/misses) are considered as low level outputs. *Cache flow non-interference* demands the changing of the cache lines accessed by the victim process (high inputs) does not affect the public observations on the cache usage (low outputs). Informally, cache flow interference happens if the usage (we focus on the accessing time) of the cache lines accessed by one victim process affects the usage of the cache lines accessed by attacker VM processes. Fig. 2 presents some intuition of the cache NI policy discussed above.

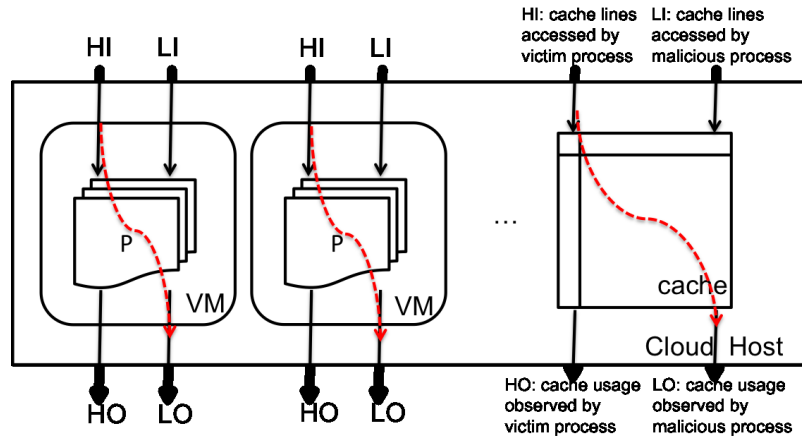


Fig. 2. Cache non-interference

Formally, the policy of flow non-interference can be considered in terms of the equivalence relations on the system behaviours from the observer's view, including the state evolution of information container and the timing behaviour of cache accessing. This is due to the fact that the system behaviours are modelled as timed runs with security classification of identifiers and with timing considerations when accessing caches during the process communications in our model.

Definition 2 (Flow security environment). Let \mathcal{L} be a finite flow lattice, \sqsubseteq denote the ordering relation of \mathcal{L} , I denote the set of VM instances running upon any host h , Ω_H and Ω_I denote a set of categories for hosts and sub-categories for instances respectively. The flow security environment is considered as:

$$\Xi : (\tau_v, \tau_c, \alpha_c, \beta_h, \beta_i),$$

where $\tau_v : \mathbf{Vars} \mapsto_{\tau_v} L$, $\tau_c : \mathbf{CLines} \mapsto_{\tau_c} L$, $\alpha_c : \mathbf{CLines} \mapsto_{\alpha_c} I$, $\beta_h : \mathbf{Hosts} \mapsto_{\beta_h} \Omega_H$, $\beta_i : \mathbf{VMs} \mapsto_{\beta_i} \Omega_I$. Furthermore, we say $\Xi \sqsubseteq \Xi'$ iff $\forall x \in \mathbf{Vars}, l \in \mathbf{CLines}$,

$i \in \text{VMs}$ and $h \in \text{Hosts}$:

$$\begin{aligned} & \Xi(\tau_v(x)) \sqsubseteq \Xi'(\tau_v(x)) \wedge \Xi(\tau_c(l)) \sqsubseteq \Xi'(\tau_c(l)) \\ & \wedge \Xi(\beta_h(h)) \sqsubseteq \Xi'(\beta_h(h)) \wedge \Xi(\beta_i(i)) \sqsubseteq \Xi'(\beta_i(i)), \end{aligned}$$

and for $t \in L$, $\omega_I \subseteq \Omega_I$, and $\omega_H \subseteq \Omega_H$, we say $\Xi \sqsubseteq (t, \omega_I, \omega_H)$ iff:

$$\Xi(\tau_v(x)) \sqsubseteq t \wedge \Xi(\tau_c(l)) \sqsubseteq t \wedge \Xi(\beta_h(h)) \sqsubseteq \omega_H \wedge \Xi(\beta_i(i)) \sqsubseteq \omega_I,$$

where we abuse notation $\Xi(\tau_v(x))$, $\Xi(\tau_c(l))$, $\Xi(\beta_h(h))$ and $\Xi(\beta_i(i))$ to denote $\tau_v(x)$, $\tau_c(l)$, $\beta_h(h)$ and $\beta_i(i)$ in environment Ξ respectively.

Definition 3 ((t, ω_I, ω_H) -equivalent configuration $=_{\Xi, (t, \omega_I, \omega_H)}$). Consider processes running upon hosts of VPN G , let Ξ be a security environment, $t \in L$ be a security level, $\omega_H \subseteq \Omega_H$ be a category and $\omega_I \subseteq \Omega_I$ be a sub-category. For any $x \in \text{Vars}$, $l \in \text{CLines}$, assume i and h are the instance and host which x, l belong to, we define store (t, ω_I, ω_H) -equivalence under Ξ as follows: $\sigma_1(x) =_{\Xi, (t, \omega_I, \omega_H)} \sigma_2(x)$ iff:

$$(\Xi(\tau_v(x)) \sqsubseteq t \wedge \Xi(\beta_i(i)) \sqsubseteq \omega_I \wedge \Xi(\beta_h(h)) \sqsubseteq \omega_H) \Rightarrow \sigma_1(x) = \sigma_2(x),$$

and cache line (t, ω_I, ω_H) -equivalence under Ξ as follows: $\delta_1(l) =_{\Xi, (t, \omega_I, \omega_H)} \delta_2(l)$ iff:

$$(\Xi(\tau_c(l)) \sqsubseteq t \wedge \Xi(\beta_i(i)) \sqsubseteq \omega_I \wedge \Xi(\beta_h(h)) \sqsubseteq \omega_H) \Rightarrow \delta_1(l) = \delta_2(l).$$

Furthermore, given two configurations $\Gamma_1 = (\sigma_1, \delta_1, i_1, h_1)$ and $\Gamma_2 = (\sigma_2, \delta_2, i_2, h_2)$, we say $\Gamma_1 =_{\Xi, (t, \omega_I, \omega_H)} \Gamma_2$ iff:

$$\begin{aligned} & (\forall x \in \text{Vars}. \sigma_1(x) =_{\Xi, (t, \omega_I, \omega_H)} \sigma_2(x)) \wedge (\forall l \in \text{CLines}. \delta_1(l) =_{\Xi, (t, \omega_I, \omega_H)} \delta_2(l)) \\ & \wedge (\beta_i(i_1) \sqsubseteq \beta_i(i_2)) \wedge (\beta_h(h_1) \sqsubseteq \beta_h(h_2)). \end{aligned}$$

Definition 4 (Strong bisimulation $\overset{s}{\sim}_{\Xi, (t, \omega_I, \omega_H)}$ and weak bisimulation $\overset{w}{\sim}_{\Xi, (t, \omega_I, \omega_H)}$). Consider two timed runs running upon host h under security environment Ξ :

$$\lambda = \langle \Gamma_0, (e_0, \Delta t_0) \rangle \rightarrow \cdots \rightarrow \langle \Gamma_n, (e_n, \Delta t_n) \rangle \rightarrow \Gamma$$

$$\lambda' = \langle \Gamma'_0, (e'_0, \Delta t'_0) \rangle \rightarrow \cdots \rightarrow \langle \Gamma'_n, (e'_n, \Delta t'_n) \rangle \rightarrow \Gamma'$$

$\forall \Gamma_0, \Gamma'_0$ such that $\Gamma_0 =_{\Xi, (t, \omega_I, \omega_H)} \Gamma'_0$, we say λ and λ' are strong (t, ω_I, ω_H) -bisimilar to each other, i.e., $\lambda \overset{s}{\sim}_{\Xi, (t, \omega_I, \omega_H)} \lambda'$, iff:

$$\forall j \in \{0 \dots n\}. (\Gamma_j =_{\Xi, (t, \omega_I, \omega_H)} \Gamma'_j) \wedge (\Delta t_j = \Delta t'_j);$$

and say λ and λ' are weak (t, ω_I, ω_H) -bisimilar to each other, i.e., $\lambda \overset{w}{\sim}_{\Xi, (t, \omega_I, \omega_H)} \lambda'$, iff:

$$(\Gamma =_{\Xi, (t, \omega_I, \omega_H)} \Gamma') \wedge \left(\sum_{j=0}^n \Delta t_j = \sum_{j=0}^n \Delta t'_j \right).$$

Definition 5 (Cache flow security policy). Given a security level $L \in \mathbb{L}$, $\omega_H \subseteq \Omega_H$, and $\omega_I \subseteq \Omega_I$ a VPN G under security environment Ξ is considered strong cache flow secure iff:

$$\forall \lambda, \lambda' \in \Lambda. (\Gamma_0 =_{\Xi, (L, \omega_I, \omega_H)} \Gamma'_0 \Rightarrow \lambda \overset{s}{\sim}_{\Xi, (L, \omega_I, \omega_H)} \lambda'),$$

where Γ_0 and Γ'_0 denote the initial configuration of λ and λ' respectively, Λ denotes all runs of components of G . Similarly, the definition of weak cache flow secure can be given.

Example 3. Consider the model presented in Example 1. Let $\tau_v(x) = \tau_v(y) = H$, $\tau_v(m_1) = \tau_v(m_2) = M$, $\tau_v(z) = L$, and $L \sqsubset M \sqsubset H \in \mathbb{L}$. Let us assume $\beta_i(\mathbf{VM}_1) = \beta_i(\mathbf{VM}_2) = \omega_I$, and $\beta_h(\mathbf{Host}_1) = \omega_H$. Communicating cache channels are thus assigned with security labels regarding the data they transmit: $\tau_c(\mathbf{CAddr}_{\text{key}}) = H$, $\tau_c(\mathbf{CAddr}_{\text{msg}}) = M$. Note that the state of variable z depends on the state of cache address of key , and is affected by the communication time for data transmission between P and Q . Therefore the model does not satisfy the cache flow security policy since for any given two runs, both the timing condition and configuration equivalent condition of $\overset{w}{\sim}_{\Xi, (L, \omega_I, \omega_H)}$ are not guaranteed to be satisfied.

In order to close the cache timing channel, we consider the communication as a scenario of sending and receiving processes running in parallel with certain time interleaving data transmission scheme:

$$\frac{\Gamma \vdash w \Downarrow v \quad w \Leftarrow \mathbf{CAddr}_a \quad a \Rightarrow \mathbf{CAddr}_a \quad t < T}{\langle \text{SLEEP}(T - t) \rightarrow P \triangleleft (t := \Delta t(a!w \parallel a?x) < T) \triangleright \text{STOP}, \Gamma \rangle} \quad (1)$$

$$\xrightarrow{a(w)} \langle P, \Gamma[\sigma(x) = v, \delta(\mathbf{CAddr}_a) = \emptyset] \rangle$$

The communicating procedure needs to complete in T time units (together with sleeping time) and then behaves as P ; the value of w is sent to variable x via channel a , channel a and the relevant cache lines are then tagged as $\tau_c(w)$. The communication will be considered as failed if T time units have passed but the communication has not completed yet. Fixed completion time T prevents the timing leakage introduced by the cache channel communication.

Example 4. Consider the model presented in Example 1, we rewrite the communicating procedure as follows:

```

x := keyGen();
SLEEP(5 - t) → P' ◁ (t := Δt(key!x || key?y) < 5) ▷ STOP
m₁ := encrypt(y, "message");
SLEEP(5 - t) → Q' ◁ (t := Δt(msg!m₁ || msg?m₂) < 5) ▷ STOP

```

The timing condition of weak (t, ω_I, ω_H) -bisimulation specified in Definition 4 is now ensured, while the configuration condition is still violated. This will be addressed in next Section.

5 Flow Security Type System for CSP_{4v}

In order to make the low observation and cache accessing time of the executions be high input independent, the variables and cache lines are associated with security labels, VMs and hosts are assigned to categories, rules (semantic + typing) are required to ensure that: no information flows to lower level objects, no cache is shared among different VM instances, processes (c.f. instances) are not allowed to move from a lower order instance (c.f. host) to a higher one, and cache related operations in communications between processes are forced to be completed in certain time, and hence the cache flow policy is enforced.

For a process P (w.r.t. a component of G), we consider the type judgements have the form of:

$$(\tau, \omega_I, \omega_H) \vdash \Xi\{P\}\Xi'$$

where the type $(\tau, \omega_I, \omega_H)$ denotes the (environment) *counter security levels* of the communication channel/variables and *and counter categories* of VMs/hosts participated in the branch events being executed for the purpose of eliminating implicit flows from the *guard*. Ξ and Ξ' describe the type environment which hold before and after the execution of P . In general, notation:

$$\Xi \vdash (\text{exp} :_{\tau_v} t_e, l :_{\tau_c} t_l, l :_{\alpha_c} i_l, i :_{\beta_i} \omega_I, h :_{\beta_h} \omega_H)$$

describes that under type environment Ξ , expression exp and (the address of) cache line l has type t_e and t_l respectively, l is allocated to VM instance i_l , instance i is assigned to a category ω_I , and host h is assigned to a category ω_H . The type of an expression including boolean expression is defined by taking the least upper bound of the types of its free variables as standard:

$$\Xi \vdash \text{exp} :_{\tau_v} t \text{ iff } t = \sqcup_{x \in \text{fv}(\text{exp})} \Xi(\tau_v(x)).$$

All memory, caches and channels written by a t-level expression becomes tagged as t-level. Let Vars_P and CLines_P denote a set of variables defined in and cache lines allocated to process P . Typing rules for processes with security configuration are presented in Table 3. Rule TSTOP for stopping a process P ensures the cache lines allocated to P to be flushed as empty with a label of system low \perp for future use. Rule for assignment TASSIGN ensures the type of variable x to be the least upper bound of the type of the assigned expression exp and the counter level τ . Rule TMOVE regarding moving a process from one instance to another enforces the type of each variable and cache line involved in process P to be the least upper bound of the type of itself and the counter level τ , and ensures its owner to be the VM identifier i' where the process is moving to, and ensures category of the moving-to-instance to be the least upper bound of that of itself and the moving-from-instance; rule TMOVE regarding moving an instance from one host h to another h' essentially moves all processes running upon the instance to h' such that each of which follows the rule of process moving. Rule for composition TSEQ ensures the typing environment in terms of the sequential event in a compositional way. Rule for sending operator TSEND ensures that the type of

| | |
|-----------|--|
| (TSUB) | $\frac{\tau_1 \vdash \Xi_1\{P\}\Xi'_1}{\tau_2 \vdash \Xi_2\{P\}\Xi'_2} \quad \tau_2 \sqsubseteq \tau_1, \Xi_2 \sqsubseteq \Xi_1, \Xi'_1 \sqsubseteq \Xi'_2$ |
| (TASSIGN) | $\frac{\Xi \vdash \text{exp} :_{\tau_v} t}{(\tau, \omega_I, \omega_H) \vdash \Xi\{x := \text{exp}\}\Xi'(x \mapsto_{\tau_v} \tau \sqcup t)}$ |
| (TSTOP) | $(\perp_{\mathcal{L}}, \perp_{\Omega_I}, \perp_{\Omega_H}) \vdash \Xi\{\text{STOP}_P\}\Xi'(\{l \mapsto_{\tau_c} \perp \mid \forall l \in \mathbf{CLines}_P\})$ |
| (TSKIP) | $(\perp_{\mathcal{L}}, \perp_{\Omega_I}, \perp_{\Omega_H}) \vdash \Xi\{\text{SKIP}\}\Xi$ |
| (TMOVE) | $\frac{\Xi \vdash (\{x :_{\tau_v} t_x, l :_{\tau_c} t_l, l :_{\alpha_c} i \mid \forall x \in \mathbf{Vars}_P, l \in \mathbf{CLines}_P\}), i :_{\beta_i} \omega, i' :_{\beta_i} \omega'}{(\tau, \omega_I, \omega_H) \vdash \Xi\{\text{MOVE}_P(i')\}\Xi'(\{x \mapsto_{\tau_v} t_x \sqcup \tau, l \mapsto_{\tau_c} t_l \sqcup \tau, l \mapsto_{\alpha_c} i' \mid \forall x \in \mathbf{Vars}_P, l \in \mathbf{CLines}_P\}, i \mapsto_{\beta_i} \sqcup\{\omega, \omega'\})}$ |
| (TSEQ) | $\frac{h : [I].M_I \quad I = \langle i : [P_1], i : [P_2], \dots, i : [P_n] \rangle}{(\tau, \omega_I, \omega_H) \vdash \Xi_1\{\text{MOVE}_{P_1}(i')\}\Xi'_1 \quad \dots \quad (\tau, \omega_I, \omega_H) \vdash \Xi_n\{\text{MOVE}_{P_n}(i')\}\Xi'_n}$ $\frac{h' : [I'].M_{I'} \quad I' = \langle i' : [P'_1], i' : [P'_2], \dots, i' : [P'_n] \rangle}{(\tau, \omega_I, \omega_H) \vdash \langle \Xi_1, \Xi_2, \dots, \Xi_n \rangle \{\text{MOVE}_I(h')\} \langle \Xi'_1, \Xi'_2, \dots, \Xi'_n \rangle (h \mapsto \sqcup\{\omega, \omega', \omega_H\})}$ |
| (TSEND) | $\frac{\Xi \vdash w :_{\tau_v} t \quad w \Leftarrow \mathbf{CAddr}_a}{(\tau, \omega_I, \omega_H) \vdash \Xi\{a!w\}\Xi'(\mathbf{CAddr}_a \mapsto_{\tau_c} \tau \sqcup t)}$ |
| (TRECv) | $\frac{\Xi \vdash \mathbf{CAddr}_a :_{\tau_c} t}{(\tau, \omega_I, \omega_H) \vdash \Xi\{a?x\}\Xi'(x \mapsto_{\tau_v} \tau \sqcup t)}$ |
| (TBRANCH) | $\frac{\Xi \vdash b :_{\tau_v} t \quad (t \sqcup \tau, \omega_I, \omega_H) \vdash \Xi\{P\}\Xi'_P \quad (t \sqcup \tau, \omega_I, \omega_H) \vdash \Xi\{Q\}\Xi'_Q}{(\tau, \omega_I, \omega_H) \vdash \Xi\{P \triangleleft b \triangleright Q\}\Xi' \quad \Xi' = \Xi'_P \sqcup \Xi'_Q}$ |
| (TLOOP) | $\frac{\Xi_i \vdash b :_{\tau_v} t_i \quad (t_i \sqcup \tau, \omega_I, \omega_H) \vdash \Xi_i\{P\}\Xi'_i \quad i = 0, \dots, n}{(\tau, \omega_I, \omega_H) \vdash \Xi\{b \triangleleft (P)^*\}\Xi'_n} \quad \Xi_0 = \Xi, \Xi_{i+1} = \Xi'_i \sqcup \Xi, \Xi_{n+1} = \Xi'_n$ |
| (TPAR) | $\frac{\begin{array}{l} (\tau, \omega_I, \omega_H) \vdash \Xi\{P\}\Xi' \quad (\tau, \omega_I, \omega_H) \vdash \Xi\{Q\}\Xi'' \\ \Xi' \vdash (\{x :_{\tau_v} t'_x, l :_{\tau_c} t'_l \mid \forall x \in \mathbf{Vars}, l \in \mathbf{CLines}\}) \\ \Xi'' \vdash (\{x :_{\tau_v} t''_x, l :_{\tau_c} t''_l \mid \forall x \in \mathbf{Vars}, l \in \mathbf{CLines}\}) \end{array}}{(\tau, \omega_I, \omega_H) \vdash \Xi\{P\ Q\}\Xi'''(\{x \mapsto_{\tau_v} t'_x \sqcup t''_x, l \mapsto_{\tau_c} t'_l \sqcup t''_l \mid \forall x \in \mathbf{Vars}, l \in \mathbf{CLines}\})}$ |

Table 3. Typing rules for processes with security configuration.

the cache channel for sending expression w is to be the least upper bound of the type of w and the counter level, and rule for receiving operator **TRECv** ensures that the type of the receiving variable x is to be the least upper bound of the type of channel and the counter level. Rule for branch event **TBRANCH** specifies that the typing environment is required to be enforced in terms of the branch

body with the counter level being the least upper bound of the current counter level and the type of the guard. Rule for loop operator TLOOP calculates the least fixed point of the type environment transition function on the security lattice. Rule for parallel operator TPAR ensures that the type of each information container (including process variables and cache lines) is to be the least upper bound after the execution of each parallel process.

In overall, the derivation rule $(\tau, \omega_I, \omega_H) \vdash \Xi\{P\}\Xi'$ ensures that:

- variables and cache lines whose final types in Ξ' are less than τ must not be changed by P ;
- the final value of a variable (or a cache line) say x whose final type is $\Xi'(x) = t$ must not depend on the initial values of those variables (or cache lines) say z whose initial type $\Xi(z)$ is greater than t .
- processes (c.f. instances) belonging to a higher order category instances (c.f. host) must not move to an instance (c.f. a host) with a lower order category.

Theorem 1 (Monotonicity of the type environment transition function). *Given L and P , for all τ, ω_I, ω_H and Ξ , the type environment transition function: $\mathcal{T}_{P,L}(\Xi, (\tau, \omega_I, \omega_H)) \mapsto \Xi'$ regarding $(\tau, \omega_I, \omega_H) \vdash \Xi\{P\}\Xi'$ is monotone.*

Proof. The proof is obtained by induction on the semantic structure of the process. Particularly, for the case of loop, the sequences of $\Xi'_0, \Xi'_1, \Xi'_2, \dots$ and $\Xi''_0, \Xi''_1, \Xi''_2, \dots$ form ascending chains with a least upper bound due to the finiteness of \mathbb{L} , so rule TLOOP calculates the least fixed point of $\mathcal{T}_{P,L}$ on \mathbb{L} . \square

Definition 6 (Semantic flow security condition). *We say the semantic relation of P satisfies $(\tau, \omega_I, \omega_H)$ -flow security property (denoted by $\phi_{\tau, \omega_I, \omega_H}$), written as: $(\Xi\{P\}\Xi') \models \phi_{\tau, \omega_I, \omega_H}$, iff:*

i) for all Γ, Γ', x and l :

$$\langle P, \Gamma \rangle \Downarrow \Gamma' \wedge \Xi' \sqsubset (\tau, \omega_I, \omega_H) \Rightarrow \Gamma(\sigma(x)) = \Gamma'(\sigma(x)) \wedge \Gamma(\delta(l)) = \Gamma'(\delta(l));$$

where we abuse notation $\Gamma(\sigma(x)), \Gamma(\delta(l))$ to denote $\sigma(x), \delta(l)$ in configuration Γ .

ii) and for all $t \in L, o \in \Omega_I, o' \in \Omega_H, \Gamma_1$ and Γ_2 :

$$\Gamma_1 =_{\Xi, (t, o, o')} \Gamma_2 \Rightarrow \Gamma'_1 =_{\Xi, (t, o, o')} \Gamma'_2.$$

We say the flow security type system is sound if the well-typed system is flow secure, more precisely, whenever $(\tau, \omega_I, \omega_H) \vdash \Xi\{P\}\Xi'$ then the semantic relation of P is flow secure.

Theorem 2 (Soundness of the flow security type system). *The type system proposed in Table 3 is sound, i.e.,*

$$(\tau, \omega_I, \omega_H) \vdash \Xi\{P\}\Xi' \Rightarrow (\Xi\{P\}\Xi') \models \phi_{\tau, \omega_I, \omega_H}.$$

Proof. Since $\tau \vdash \Xi\{P\}\Xi'$ ensures that: for all variables and cache lines x , whenever $\Xi'(x) \sqsubset \tau$ then there are no assignments to x in P , and thus i) is clearly satisfied; and for any variables y , such that $\Xi(y) \sqsubset \Xi'(x)$, the final value of x does not depend on the initial values of y , we can then prove for all $t \in \mathbb{L}$, $o \in \Omega_I$, $o' \in \Omega_H$, configurations Γ and Γ' such that $\langle P, \Gamma \rangle \Downarrow \Gamma'$, whenever $\Gamma_1 =_{\Xi, (\tau, \omega_I, \omega_H)} \Gamma_2$ then $\Gamma'_1 =_{\Xi, (\tau, \omega_I, \omega_H)} \Gamma'_2$, by induction on the structure of the derivation tree. \square

Theorem 3 (Flow secure of communications). *Given a CSP_{4v} model \mathbf{A} , for all P running upon any VM i of any host h in \mathbf{A} , if $(\Xi\{P\}\Xi') \models \phi_{\tau, \omega_I, \omega_H}$, then \mathbf{A} is weak cache flow secure with $L = \tau$.*

Proof. The proof includes two parts in terms of the definition of weak cache flow security policy given in Definition 5: channel of timing observable behaviours of victim process, and channel of observable low outputs influenced by high inputs. The first part is ensured by the semantics of communications specified in (1), which must be completed in certain time, and the second part is ensured by the soundness of the type system presented in Theorem 2. \square

Example 5. Consider again the model presented in Example 1 and 3. It is clear that $(\tau, \omega_I, \omega_H) \vdash \Xi\{R\}\Xi'$ does not hold since the assignment to z make $\Xi'(z) > \Xi(z)$; while $\Xi\{R\}\Xi' \models \phi_{\tau, \omega_I, \omega_H}$ holds if the communication between P and Q fails and $\Xi\{R\}\Xi' \not\models \phi_{\tau, \omega_I, \omega_H}$ holds otherwise.

6 Related Work

This paper relates to the topic of information flow analysis in virtualised computing systems from perspective of formal languages with a concern of cache timing attacks.

Cross-VM side-channel attacks in virtualised infrastructure allowed the attacker to extract information from a target VM and stole confidential information from the victims [24,32,33]. Over the last decade, there have been sustained efforts in exploring solutions to defend cache channel attacks in virtualised computing environment via the approaches of *cache partition* at either *hardware-level* [30,31,6,15] or *system-level* [21,26,14,34,17], and the approaches of *cache randomisation* via introducing randomization in cache uses through either new *hardware design* [29,30,31,18,16,23] or *compiler-assistant design* [7,16,4,22]. Wang and Lee [30] identified cache interference as the main cause of different types of cache side channel attacks. Security-aware cache designs were proposed to mitigate the cache interference issue: Partition-Locked cache (PLcache) eliminated cache interference via preventing cache sharing in a flexible way, and Random Permutation cache (RPcache) allowed cache sharing but randomised cache interference so that no information can be deduced. More recently, Liu et al. [17] developed CATalyst to defend cache-based side channel attacks for the cloud computing system. Specifically, CATalyst used Cache Allocation Technology (CAT) on Intel processors to partition the last-level cache into secure and

non-secure partitions. The secure partition was loaded with cache-pinned secure pages and was software-managed, while the non-secure partition can be freely used by any applications and kept hardware-managed. Security-sensitive code and data can be loaded and locked by users via mapping them to the cache-pinned pages. Thus a hybrid hardware-software managed cache was constructed to protect the sensitive code and data. However, these efforts mostly require significant changes to the hardware, hypervisors, or operating systems, which make them impractical to be deployed in current cloud data centres. Formal treatment on flow security policies upon side-channel attack detection, leveraging program analysis techniques and relevant tools are still needed in order to improve the accuracy and applicability of leakage analysis and control in the virtualised infrastructure. In this paper, we address the flow security issue in virtualised computing environment from perspective of *programming language* and *program analysis* techniques.

On the other hand, there have been lasting investigations on flow property specification and enforcement via approaches of *formal language and analysis*. The conception of information flow specifies the security requirements of the system where no sensitive information should be released to the observer during its executions. Denning and Denning [5] first used program analysis to investigate if the information flow properties of a program satisfy a specified multi-level security policy. Goguen and Meseguer [8] formalised the notion of absence of information flow with the concept of non-interference. Ryan and Schneider [25] took a step towards the generalisation of a CSP formulation of non-interference to handle information flows through the concept of process equivalence. Security type systems [28,19,11,20,12,2,13] had been substantially used to formulate the analysis of secure information flow in programs. In addition to type-based treatments of secure information flow analysis for programs, Clark *et. al* presented a flow logic approach in [3], Amtoft and Banerjee proposed a Hoare-like logic for program dependence in [1]. Hammer and Snelting [9] presented an approach for information flow control in program analysis based on program dependence graphs (PDG). Based on [9], [27] extended the PDG-based flow analysis by incorporating refinement techniques via path conditions to improve the precision of the flow control. Such PDG-based information flow control is more precise but more expensive than type-based approaches. However, none of the above works has addressed the issue of flow analysis in virtualised computing systems regarding observations on both executions of communicating processes and affections of cache timing channels.

7 Conclusions

We have proposed a language-based approach for information leakage analysis and control in virtualised computing infrastructure with a concern of cache timing attacks. Specifically, we have introduced a distributed process algebra with processes able to capture flow security characters in a virtualised environment; we have described a cache flow policy for leakage analysis through communica-

tion covert channels; and we have presented a type system of the language to enforce the flow policy. In our future work, we plan to derive concrete implementation of our approach and to extend the current model to define and enforce more practical security policies.

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